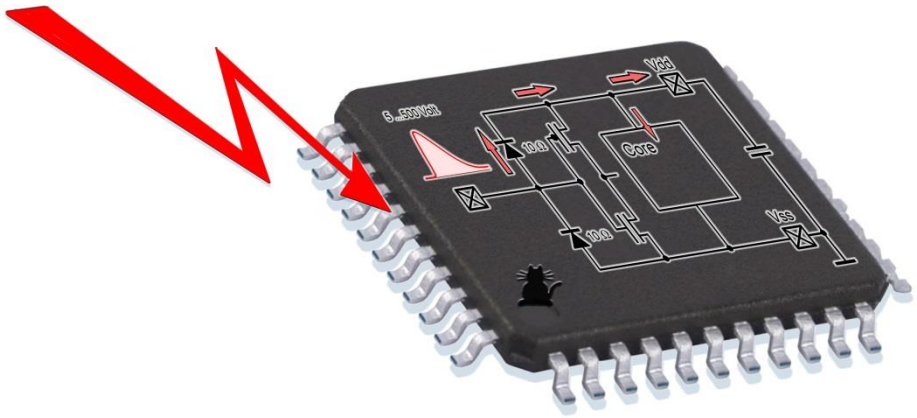
LANGER
EMV-Technik

GUIDELINE
IC EFT Immunity



Frank Deter
Gunter Langer, Langer EMV-Technik GmbH
Sven König, Langer EMV-Technik GmbH

CONTENT

page

1 GENERAL DESCRIPTION

1.1 Objective

Apart from its layout and housing design, the characteristics of the ICs which are used in a device are decisive for its EMC characteristics. The ICs susceptibility to disturbances increases significantly due to a reduction of their structural dimensions, operating voltages and operating points. The disturbance immunity is reduced to around 10 % of former ICs if the 100 nm world is approached or entered. This tendency is also reflected by the device behavior.
Given identical functionality, a product's good EMC characteristics give manufacturers an edge over competitors. The objective is thus to determine those parameters which are decisive for disturbance immunity and allow the engineers to draw conclusions for chip design.
From the user's point of view, it stands to reason to compare different IC types under the conditions which prevail in his applications.

Current common IC test procedures

Today it is common practice with electronic components (ICs, transistors) to indicate a value of one to several kV with reference to the human body model as ESD immunity in specifications. A 100 pF capacitor which is charged to the test voltage is discharged to the DUT via 1500 Ohm. This test model is described in the MIL-STD-883G and IEC 801-2 standards. The machine model is another test model based on the same principle.
The test is exclusively used to ensure a certain stability of the IC to destruction when handling the component during manufacture, packaging, transport and assembly. The test object is, however, not connected to the power supply and thus not in operation.
The ESD immunities specified according to the human body model are not related to the ESD behavior in operation. The protective mechanisms which are designed for the human body model may even cause problems in disturbance operating tests (without taking into account any disturbances in operation).

This approach means that a clear line has to be drawn between the objective of the present directive and that pursued by the test system from Langer EMV-Technik.

IC test system from Langer EMV-Technik

This test system refers to the ESD and burst immunity of PCBs and electronic devices. These are subjected to an ESD and burst test (IEC standard 61000-4-2/61000-4-4). The test voltages are in the kV range. The ICs themselves have considerably lower disturbance levels.
The pulsed voltages which are applied to the device from outside are attenuated on their way to the IC. Voltages of several kV outside of the device are thus reduced to around 1 ... 100 V on the IC pin.

The I**C test system** has been developed to test the IC immunity to pulsed disturbances.

The IC test system permits the

- user of ICs:
    - to keep track of changes in disturbance immunity
    - to take control over component selection and layout
    - to make decisions on where to use the IC

- manufacturer of ICs:
    - to check the immunity of existing ICs to disturbances
    - to identify the causes of disturbances and improve the IC

1.2 Set-up of the IC test system

An RF-proof IC (DUT) connection is the basic requirement for correct measurements. A solid ground plane is thus used as a reference plane in which the DUT is inserted using an IC test board (Figure 1) which has a continuous ground plane too.
The respective measuring task determines which of the different probes is used for the actual measurement. The probe is positioned so that a large part of its surface rests on the ground plane and thus provides an electric connection. The measuring connection is established to the DUT pin under test via the probe's pin contact. This confined set-up and the continuous ground plane ensure that correct measurements can be performed up to and even in the GHz range.

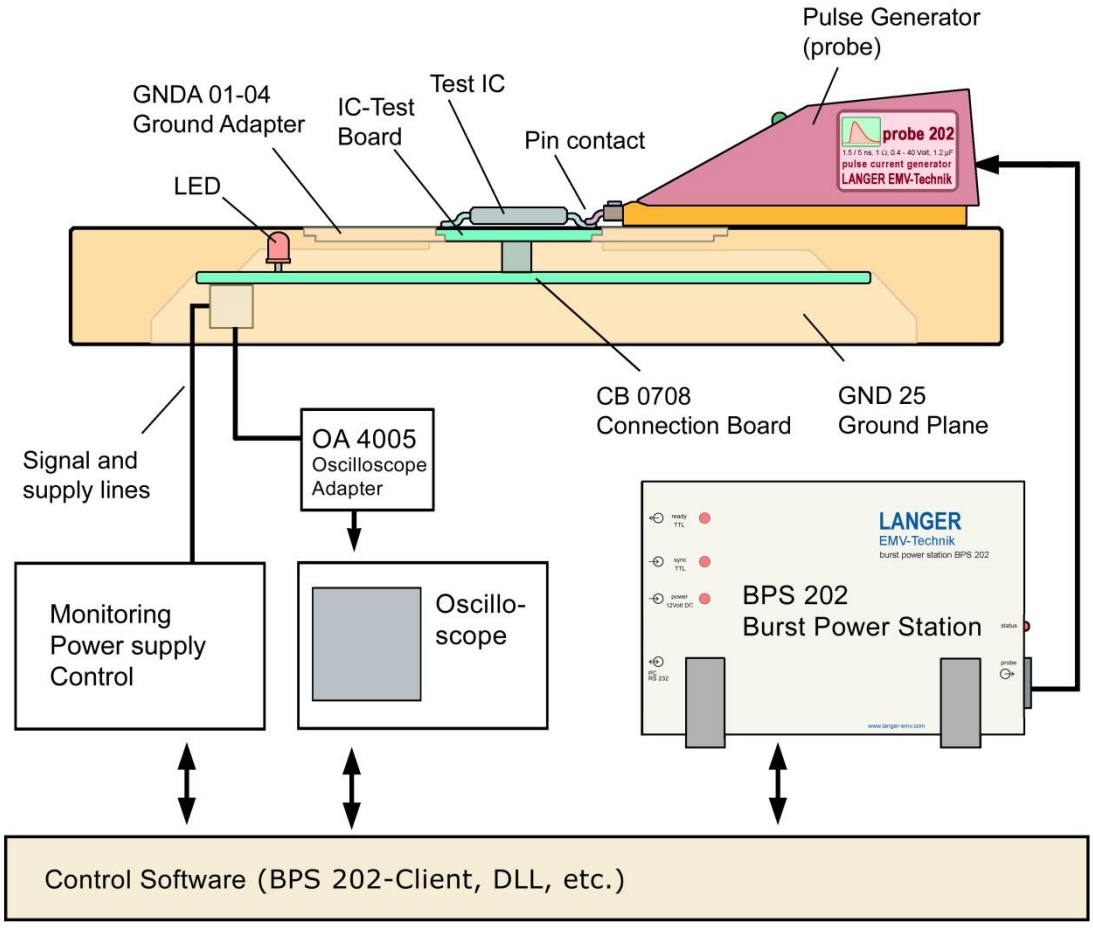


Figure 1 - test set-up

The measurement system comprises the following components:

1. GND25 Ground Plane including GNDA Ground Adapter and CB 0708 Connection Board
2. IC Test Board (must be manufactured for the respective IC types)
3. BPS 202 Burst Power Station) for control
4. P202 / P302 probes for conducted disturbances
5. Operating software for the PC

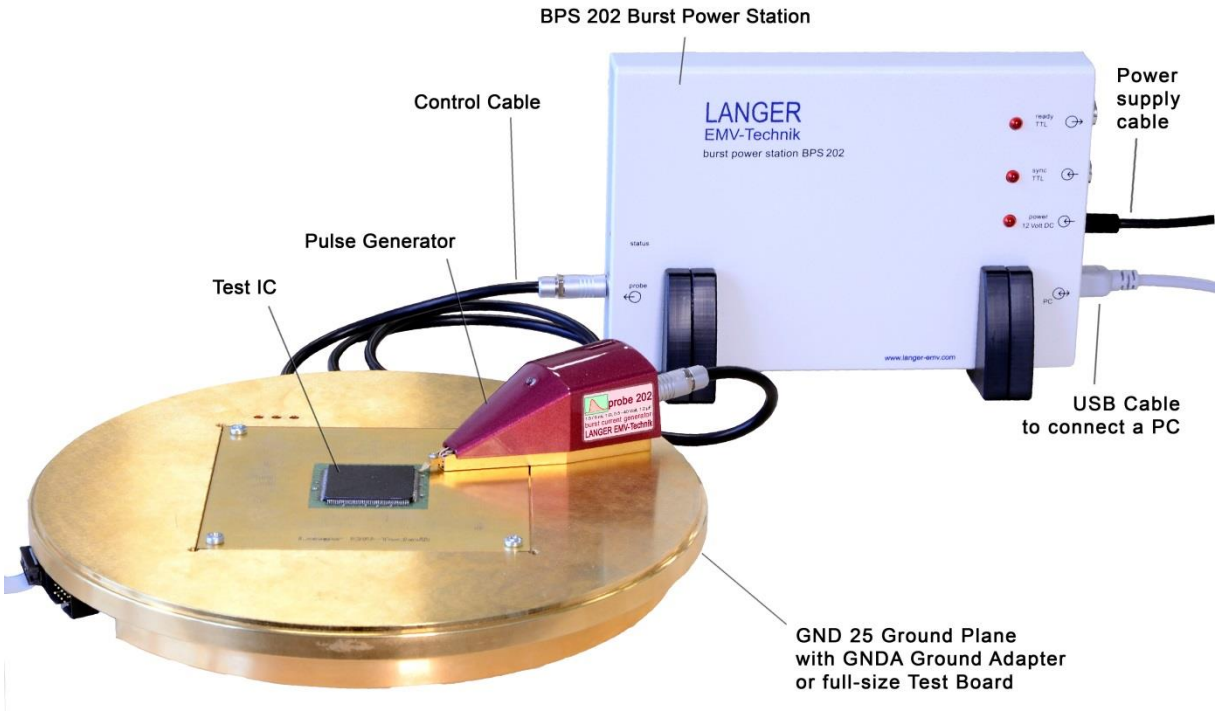


Figure 2 - components of the IC test system

The IC test board must be manufactured before measurements can be performed on an IC. This test board has several tasks:

1. A continuous contact with the ground plane must be ensured to guarantee correct measurements.
2. The supply voltage must be connected depending on the measuring task and blocked in a defined way by filter elements.
3. The relevant signals must be provided or read out to ensure the IC's function. The lines required for this purpose must be equipped with appropriate filters.

The IC test board is plugged onto the connection board. The various ports of the IC under test are supplied with power and monitored / controlled via this connection board and connecting cables.

1.3 Definition of test pulses

The IC test pulses are defined on the basis of the device test procedures. The respective test set-ups generate electric and magnetic fields in the device. These quantities also have a local effect at the interface to the IC housing. IC test generators must provide a universally applicable simulation of these electric and magnetic quantities. Figure 3 shows the set-up principle of a burst or ESD test-bench. The test pulse $u_G(t)$ which is applied to the DUT generates a current pulse i(t) which flows through the device. A voltage drop $\Delta u(t)$ occurs in the device. The voltage $\Delta u(t)$ results in an electric field strength E(t) in the device. The pulsed magnetic field H(t) which is generated in the device results from the current i(t). These fields have an indirect effect on the IC via the conductor runs connected from outside or a direct effect on the IC housings.

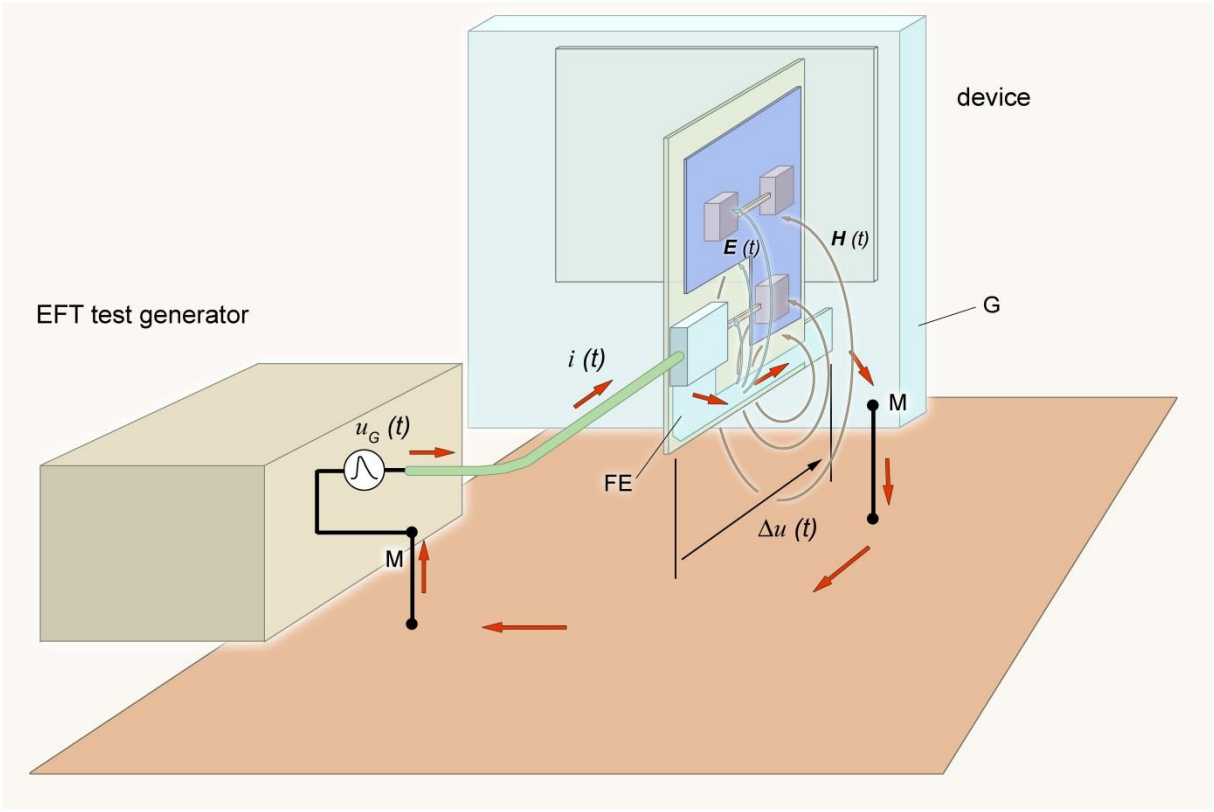


Figure 3 - set-up EFT test-bench

1.3.1 Magnetic coupling

A pulsed disturbance current which flows through a PCB generates pulsed magnetic fields. These magnetic fields B_{St} can couple into conductor loops and induce disturbance voltages u_{St}. There are two ways on which such a pulsed magnetic field can interfere with the IC function (Figure 4):

a) The induced voltage influences the IC pin which has been selected as the input. The disturbance voltage u_{St} is converted into a disturbance signal in the IC by the input circuit and further processed like a logical signal.

b) The induced voltage drives a disturbance current i_{St} into the IC pins. This disturbance current is driven directly to the IC's internal Vdd / Vss system if these are Vdd / Vss pins. However, it can also penetrate via signal pins and be guided to the IC's internal Vdd / Vss-System via internal drivers or damping diodes or capacitance. The Vdd / Vss system conducts the disturbance current to other functional components of the IC so that disturbances can occur in areas which have no functional connection to the affected pins.

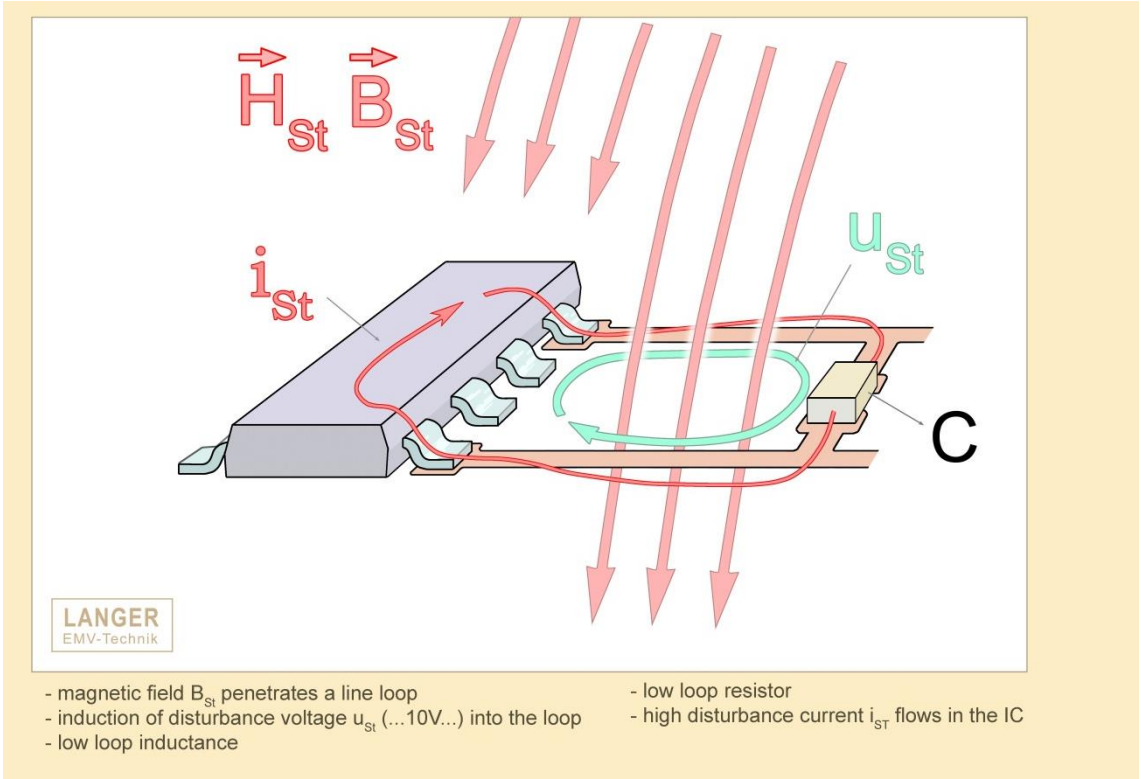


Figure 4 - influences with pulsed magnetic fields

1.3.2 Electric coupling

Assemblies can be subjected to pulsed electric fields of several 10,000 V/m (measurement set-up acc. to IEC 61000-4-4). The PCB's conductor systems receive this field (Figure 5).
A displacement current D flows to the environment via the conductor's parasitic capacitance. The IC which is connected to the lines can be interfered with in two ways:

a) Essentially, the conductor system has R and L switch elements as well as diodes against Vdd and Vss on the PCB and in the IC. The displacement current generates a disturbance pulse u_{St} on these elements. This disturbance pulse is converted into a disturbance signal by the IC's input circuit and further processed like a logical signal.

b) The displacement current is divided into two shares. A first share drains via the PCB's equivalent elements and any anti-interference capacitors that may be present. The second share of the disturbance current i_{St} flows through the IC to the Vdd / Vss system via the drivers or damping diodes. It generates an effect that is similar to that of magnetic field coupling.

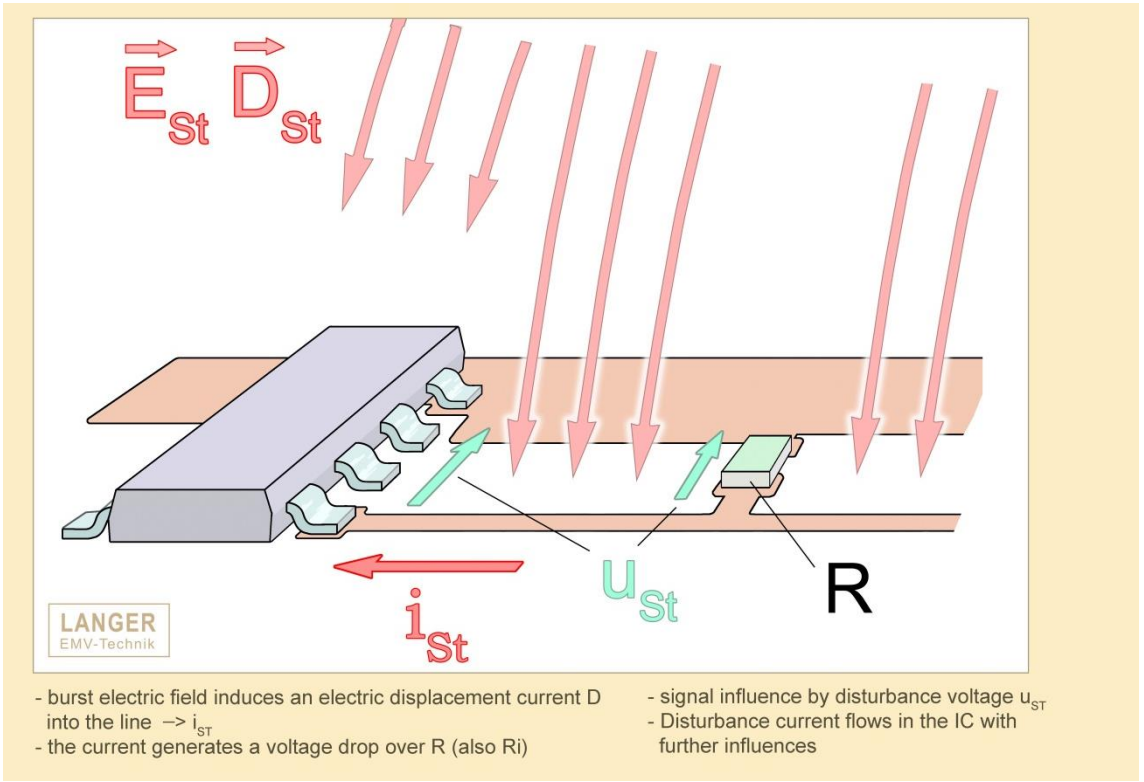


Figure 5 - influences with pulsed electric fields

1.4 Test pulses and test generators

The probes P202 and P302 are provided for disturbance pulse coupling. Their dimensional design is adapted to the mechanisms used for coupling pulses into the electronic assemblies. The P202 is provided for generating disturbances by pulsed magnetic fields. This probe has a higher coupling capacitance then the P302 and a much lower resistance.
For simulation of the electric field coupling the probe P302 is provided.
The probes are supplied and controlled by the BPS 202 burst power station.

1.4.1 Test generator with low impedance

The probe P202 is provided for generating this type of pulses (Figure 6). This probe must simulate the induction loop of the PCB. In extreme cases, this induction loop may comprise the IC's internal current path and a blocking capacitor which is connected to the pins.
The equivalent circuit of the entire current loop can have several hundred mΩ and some nH. The probe is thus designed to have a low resistance and low inductance (1 Ω, 2 nH).
The generator voltage value which is set on the PC corresponds to the disturbance effect of the probe in no-load operation. Figure 6 shows a voltage pulse which has been coupled into different loads via a P202 probe.

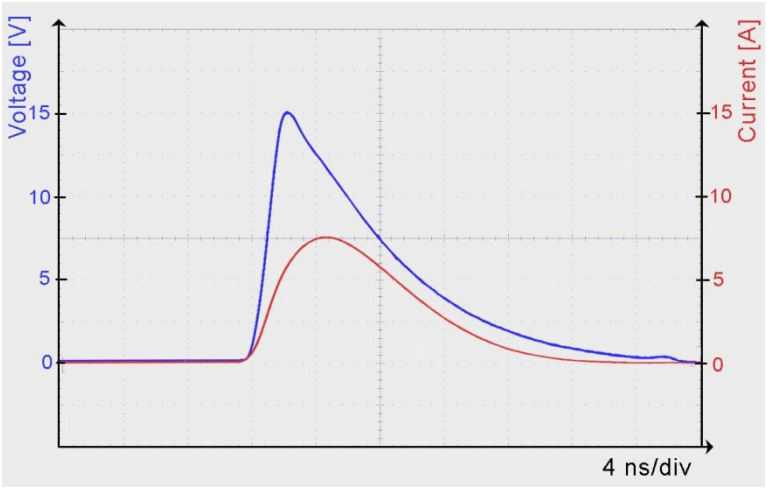


Figure 6 - P202 no-load voltage pulse (blue) and voltage on 1Ω load (red)

Technical parameters:

Probe:	**Probe 202**
Pulse shape:	1.5 / 5 ns
Coupling capacitance:	1.2 µF
Internal resistance:	1 Ω
Internal inductance:	approx. 2 nH
Pulse voltage:	± 0.4 - 40 Volt

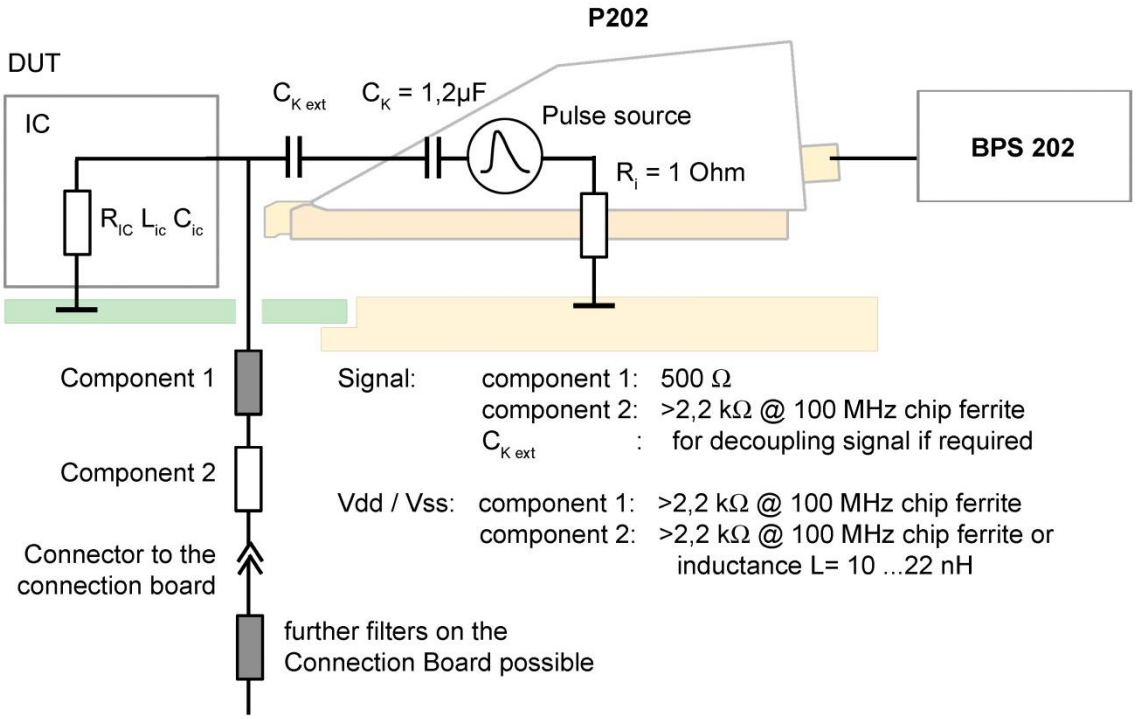


Figure 7 - generator parameters P202

1.4.2 Test generator with high impedance

The probe P302 simulates the displacement current coupling of the electric field. The probe couples voltage pulses (Figure 8) with a rise time of 1.5 ns that originate from a coupling capacitance of 20 pF into the IC. In general, the voltage pulses are short-circuited in the IC against Vdd / Vss via clamping diodes or other protective elements. The generator functions as a pulsed current source. The current pulse (Figure 8, red curve) depends on the generator parameters.

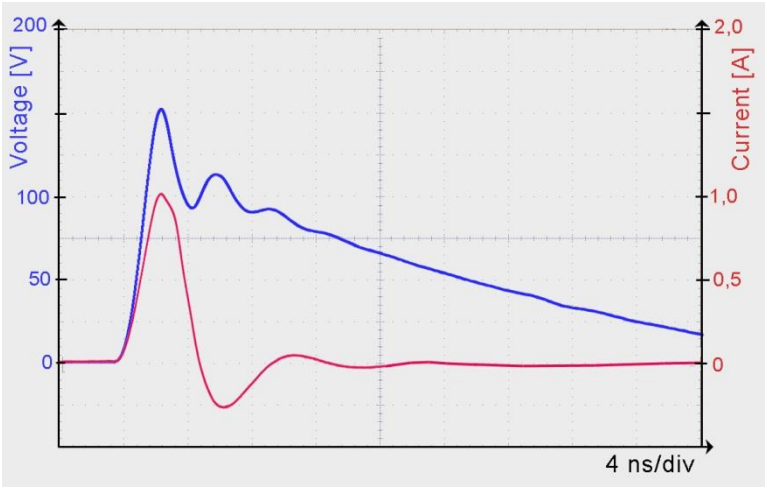


Figure 8 - P302 no-load voltage pulse (blue) and voltage on 1Ω load (red)

Technical parameters:

Probes:	**Probe 302**
Pulse shape:	1.5 / 20 ns
Coupling capacitance:	20 pF
Internal resistance:	150 Ω
Internal inductance:	approx. 50 nH
Pulse voltage:	± 5 - 500 Volt

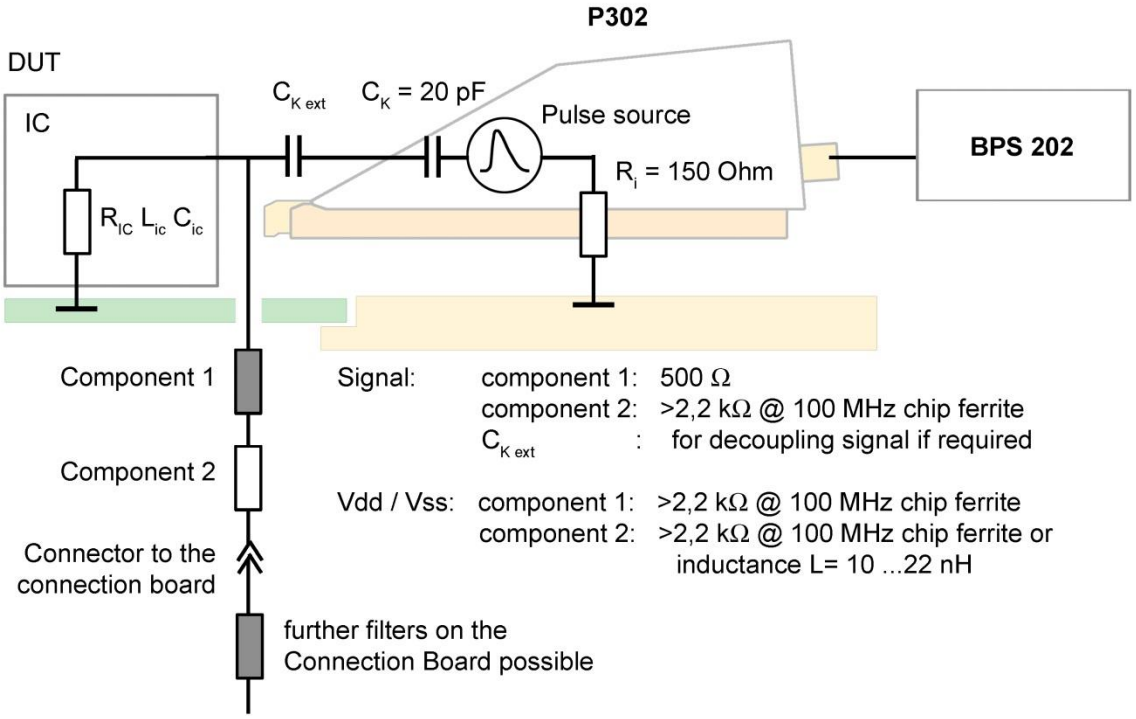


Figure 9 - generator parameters P302

2 SOFTWARE

2.1 General

The software determines the immunity of integrated circuits against EFT in a consistent manner with the following targets:

- select the suitable IC for the intended design
- identify the most sensitive pins of the IC for further consideration during the design of the electronic
- compare the performance of IC's from different manufacturers
- determine performance changes of an IC after a die shrink
- check if the performance of mass produced parts is identical to the performance of the previously tested samples

The detection of the EFT is supplied by software and hardware indicators.

ATTENTION! - The Watchdog-functionality should be switched off.
- All unused GPIOs should be configured as input with enabled internal pull-up resistor.

2.2 Equipment

- Assembler or compiler for the target microcontroller
- Programmer for the target microcontroller

2.3 Definition of failures

A failure is defined as the inability of the microcontroller to reliably read or write data to RAM, registers or on-board EEPROM. A failure is also defined as the inability to properly execute instructions. An I/O port failure is the failure of a configuration or data direction register in retaining the correct data. Inability to properly read input pins is not considered a failure.

Types of failures

- distortion of signals (e.g. signal level limits)
- fault of internal functions (e.g. of state machines)
- global failures (e.g. Reset, clock, power supply)
- changes of register data
- fault of timing, loss of synchronization, Jitter
- wrongly changes of modes
- fault due to protection clamps
- Latch up
- increased current consumption (temporarily or permanently)
- current leakage
- permanent damage

Effect of serveral failures

Generally there can be more than one failure which occurs during EFT injection. It is important to distinguish and to log the different failures. After the first failure occurs the voltage should be further increased up to the next failure or the maximum voltage level.

1. Software failure indicators

2. Hardware failure indicators

Furthermore the software must provide the following Hardware failure indicators:

- indicator of internal RESET
- indicator of port tristate

2.4 Detection of failures

2.4.1 Software failure detection

The test software must cover the critical functions of the microcontroller, such as memory access and core operations.

Different software failure detectors to test the functionality of the IC:

- "Heartbeat LED" as indication that the software is still running
- Output of an internal clock or something else as a clock monitor
- "Failure LED" should light up if any abnormal operations of the MCU are detected. This LED or digital output (for monitoring with scope) should indicate several error conditions with different blinking frequencies or error codes for example.

Caution!
While writing this software, the hardware should be considered as NOT reliable! Abnormal behavior of the hardware should be detected and stop the program or light up the Failure LED.

It is impractical to write this test in C, or any other high level language. Assembly coding should be used because the engineer needs control over which RAM addresses and registers are being used at any part of the test.

“Heartbeat LED”

The “Heartbeat LED” should be toggled every time the test loop has been executed. For better visibility the blinking frequency should be stretched to approximately 10 Hz.
If a failure is detected the “Heartbeat LED” should not stop toggling as an indicator for an independent error handling.

“Clock monitor”

The “Clock monitor” should indicate the internal clock functionality. It should put out the internal mainclock, a PLL direct or divided (e.g. PWM with a duty cycle of 50%, SPI clock...).

"Failure LED"

As an option the "Failure LED" should indicate several error conditions (see above) with different blinking frequencies or error codes (PWM, square pulse coding). The LED should be reseted by toggling the power supply off and on.

Failures to detect:

- RAM data corruption
- ROM (FLASH) data corruption
- EEPROM data corruption
- Control Register data corruption, such as Program Counter, Stack Pointer, and Data Direction Registers
- Working Register data corruption, such as the Accumulator
- Memory Address Bus error
- Memory Data Bus error
- Reset Detection
- Unexpected Interrupts or Failure to Interrupt
- Watchdog timer overflow
- Any other feature of the device that has a failure mode

Specific tests:

Program Memory
The program memory should be read up to the last location where the checksum is stored. If the least significant byte of the sum of the program memory is different from the checksum, an error should be indicated. The unused memory should be filled with NOP's and jump to a location that will signal an error.

Data Memory
The data should be tested by writing a varying pattern such as 1's and 0's, alternating 1010…, then 0101.... After each pattern is written the data should be read back and any errors should be indicated.

EEPROM should be tested in the same way as the data memory, with special attention to the write time specifications.

The *working registers* should be tested in the same manner as the Data Memory.

The *control registers* should be initialized then read back continuously and compared to the initial value. Occurring errors should indicate an error condition on the LED display.

Memory Address Bus
Use a method that tests for free toggling of each address line. Toggle one line at a time and verify that no other lines are changing.

Memory Data Bus
This is tested inherently when Program Memory is tested.

Reset Detection
Many microcontrollers have Reset status registers. If a Reset occurs, this register can be tested to see what caused the Reset including a watchdog timer overflow.

Unexpected Interrupts or failure to interrupt
If the interrupts are turned off any interrupt indicates an error.

The *timer interrupt* hardware can be tested by setting up a timer interrupt. Its operation is verified by putting a counter that is incremented every cycle of the main loop. If the timer interrupt occurs, it will clear the check timer. If an error condition exists where the interrupt doesn't happen the check timer will overflow and indicate an error on the LED display.

Watchdog Timer
The timer should be started during initialization and periodically be updated in the main loop. Any failure causing a watchdog timer overflow will be indicated by a Reset.

Failure display

There are several software failure indicators to control the proper function of the DUT:

- Failure detector: "Heartbeat LED"
- Failure detector: "Clock monitor"
- Failure detector: "Failure LED"

2.4.2 Hardware failure detection

There are several hardware failure detections to control the function of the DUT. For these failure detections software support is needed.

- Failure detector: internal RESET
- Failure detector: Tristate gathering with scope

Detector for internal RESET

Design: A logical high- or low-level is applied to an input pin via an external switch. A output pin should overtake the applied level after a RESET and visualize it with an LED.

Program: After a “RESET by hand” or a power-on-RESET the state of the input pins must be saved. The saved state is switched to an output pin.

Function: Before the evaluation the state of the external switch is toggled. In the case of an internal RESET the toggled level is output to the LED. So an internal Reset is recognized.

Tristate gathering with scope

Design: An I/O pin is set to low with a pull-down resistor and observed with a scope.

Program: The used I/O pin should be defined as an output pin and must output a high level.

Function: In case of a malfunction and restart of the software the pin is switched to tristate. The pull-down resistor pulls the pin to low level. This level change can be detected with the scope.

All unused I/O pins should be configured as an input pin with enabled internal pull-up resistor if possible.

3 HARDWARE

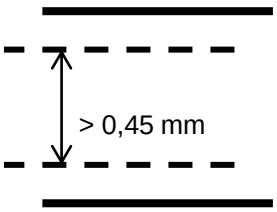
3.1 IC Test Board set-up

Size: The size of the IC test board depends on the size of the tested IC:

1. 22.7 mm x 22.7 mm (± 0.1 mm) with one connector
2. 32.7 mm x 32.7 mm (± 0.1 mm) with one or two connectors

Height: 1 mm (-0.1 mm) without solder resist

Layer design: 4 layer



top-layer – GND and the IC
layer 1 – GND (closed), without signals
layer 2 – signals without GND
bottom-layer – GND, signal and electronic components

Layer without GND must have a minimum distance of 1,1 mm to the border of the adapter board.

Surface: chemical Ni/Au

Example:

Figure 10 - Typical stackup for a test board of 1 mm thickness

Dimensions: top view (with two connectors on bottom layer)

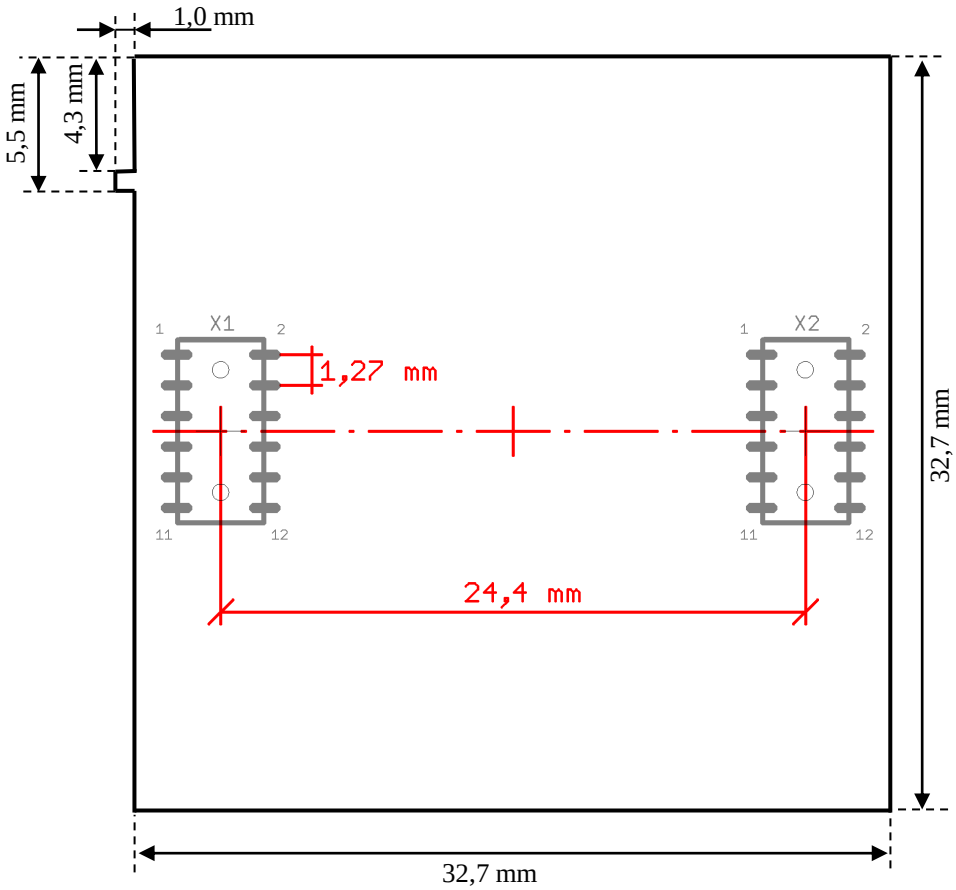


Figure 11 - position of two connectors on bottom layer

Connector: CLP-106-02-G-D-A by SAMTEC (for GND22 or older)
FLE-106-01-G-DV-A by SAMTEC (for GND25)

a) pin assignment (example for two connectors):
placed symmetrical to the middle of the bottom layer (see above)

X1

GND	1	2	GND
VCC	3	4	RESET (IN)
NC	5	6	VDD Reg/Core (optional)
NC	7	8	Failure detector 3 (IN)
NC	9	10	NC
GND	11	12	GND

X2

GND	1	2	GND
(OUT) Failure detector 1	3	4	VCC
(OUT) Failure detector 2	5	6	NC
(OUT) Failure detector 3	7	8	NC
(OUT) Failure detector 4	9	10	NC
GND	11	12	GND

b) *pin assignment (example for one connector):*
centered on bottom layer

X1

NC	1	2	GND
(OUT) Failure detector 2	3	4	Failure detector 4 (OUT)
(OUT) Failure detector 1	5	6	Failure detector 3 (OUT)
(IN) Failure detector 3	7	8	RESET (IN)
NC	9	10	VDD Reg/Core (optional)
GND	11	12	VCC

The outputs (OUT) are connected with LEDs or a scope. The inputs (IN) are connected with a switch panel.

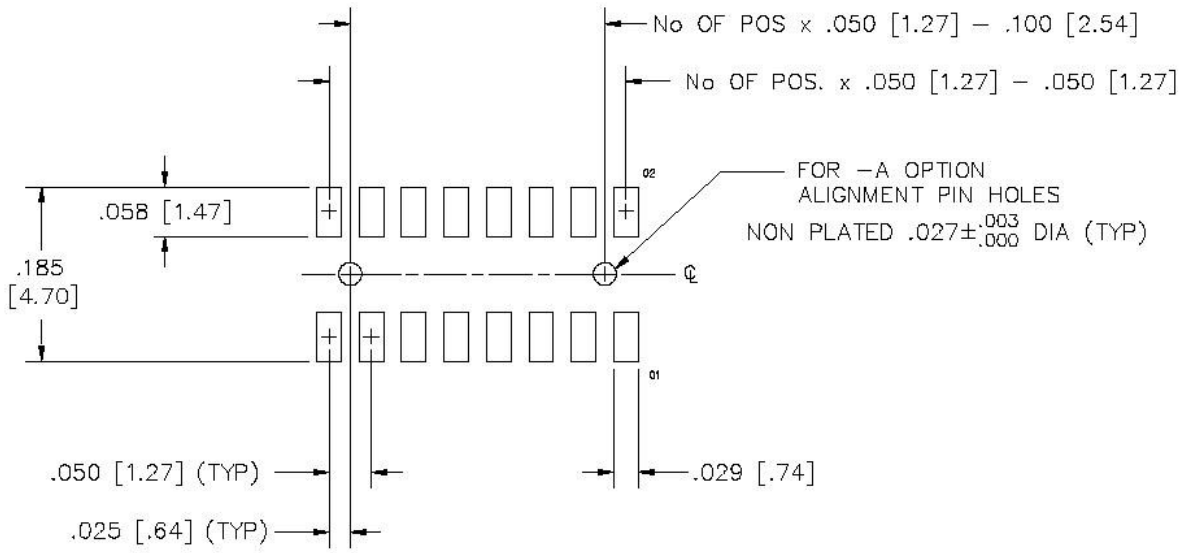


Figure 12 - footprint SAMTEC

3.2 General design rules

Top layer:

1. IC on top layer (centered), pin 1 normally upper left
2. wires < 5 mm to the filter components on the bottom layer
   (the vias should be in the pad of the pin, if possible)
   2.1 two vias for pins which are connected to GND soldering bridge or capacitors
3. closed GND area also under the IC, 4 mm in front of the pin without solder resist
4. GND vias and edge plating
5. pads to contact the pins
6. positioning marks for automated testing

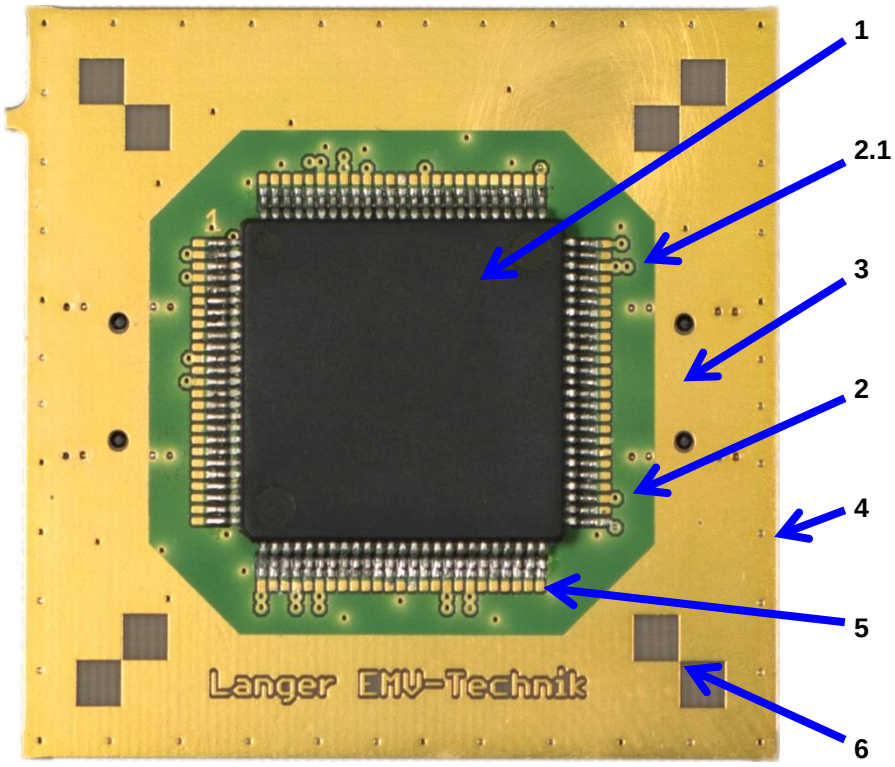


Figure 13 - example top layer

- no other vias than GND in the area without solder resist
  → shorted circuit possible caused by the test probe

layer 1:

- closed GND area

layer 2:

- without GND
- no signal under the filtering components
- vias (no GND) between layer 2 and bottom as blind vias, other vias have to be placed under the IC housing or under solder resist

Bottom layer:

7. closed ground border without a solder resist (width: minimum 1.1 mm), vias with a distance of 3 mm
8. edge plating
9. no GND and no signal lines under the filter components
10. filter elements have to be placed on the bottom next to the vias of the pins
11. position of the connector on the bottom layer
12. GND soldering bridge

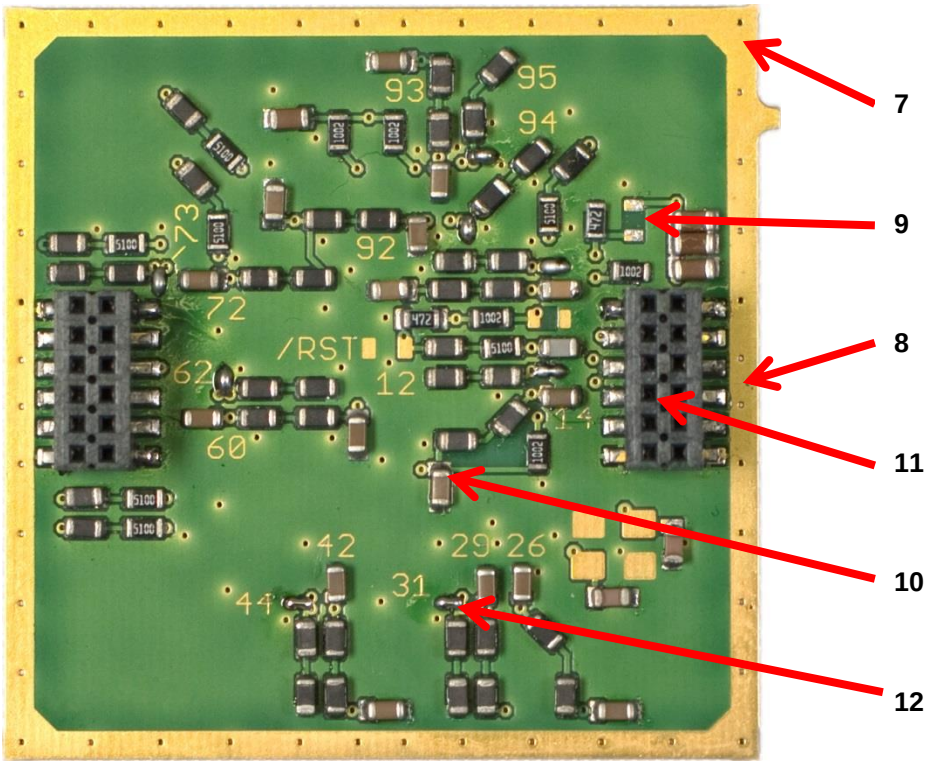


Figure 14 - example bottom layer with 2 connectors

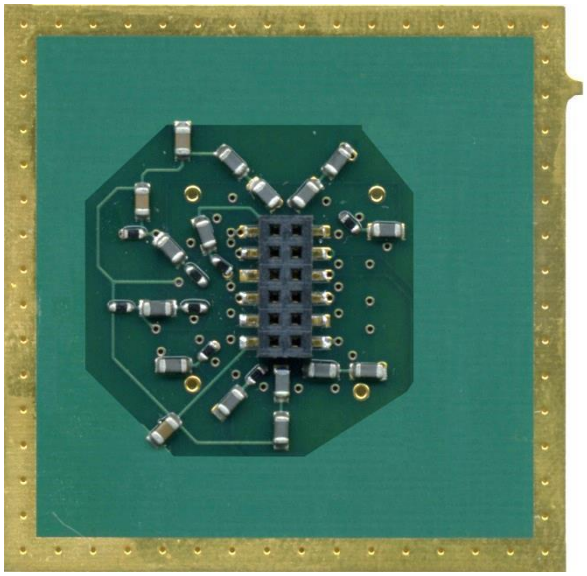


Figure 15 - example bottom layer with one connector

3.3 BGA package test

- the IC **[1]** will be placed on bottom layer, also the filter elements **[2]** and the connectors **[3]**
- pads for the balls of the IC to the contacting matrix **[4]** on top layer are conducted with vias (as short as possible)
- GND soldering bridge **[5]** or bypass capacitor can be placed also on top layer if needed
  → the contacting to the pad of the pin must be guaranteed

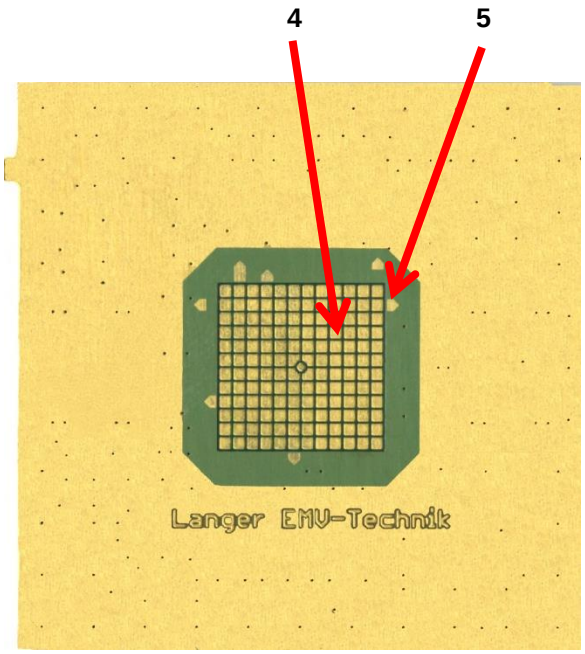


Figure 16 – example top layer BGA design

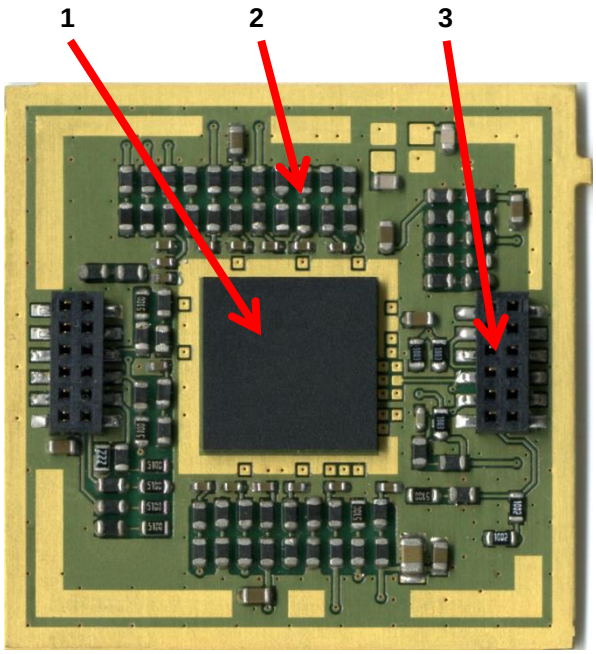


Figure 17 – example bottom layer BGA design

3.4 Supply

- bypass capacitor set-up as advised by the manufacturers
- the vias to bottom layer should be in the pad of the pin
- bypass capacitor of Vdd is next to the pin on the top layer (during the test of this pin with EFT the capacitor have to be removed)
- soldering bridges of Vss have to be placed on the top layer
- filter: chip-ferrite 2.2 kΩ at 100 MHz or higher

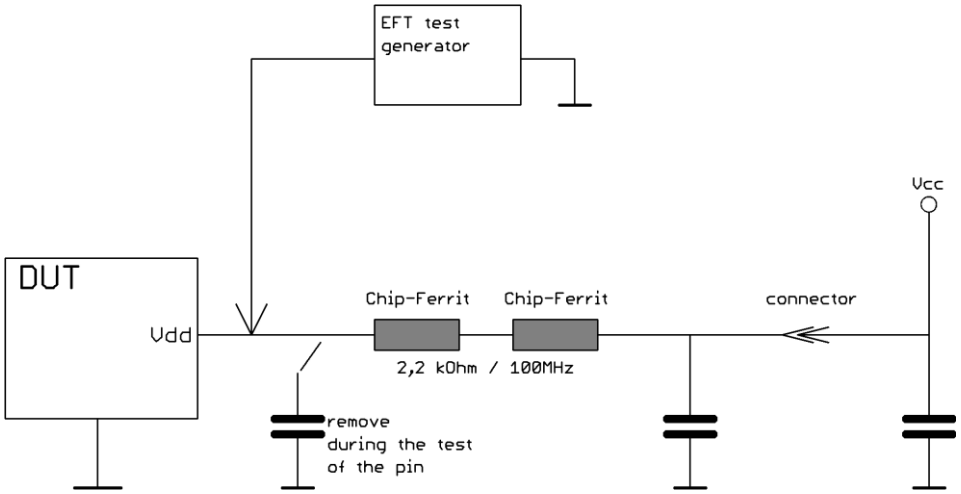


Figure 18 - example of the external set-up on Vdd

Removing the bypass capacitor and inserting filter elements prevents leading the disturbance. The bypass capacitor is substituted with the capacitor inside the probe.

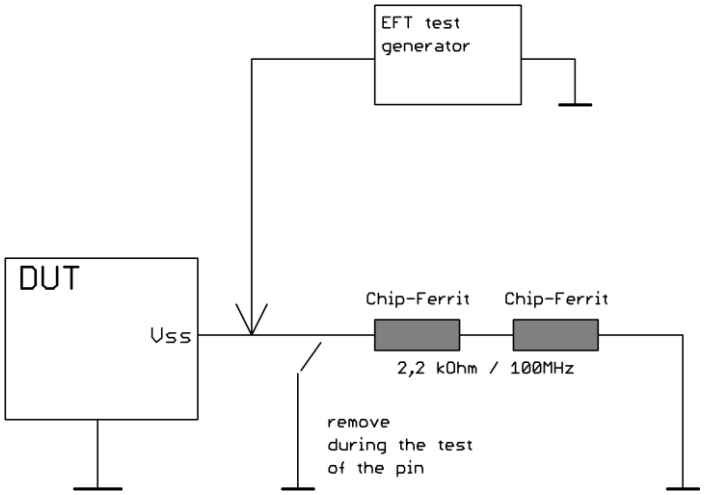


Figure 19 - example of the external set-up on Vss

Removing the GND bridge and insetting filter elements prevents leading the disturbance.

3.5 Signal lines

- filter: chip-ferrite 2.2 kΩ at 100 MHz or higher
  resistor R ca. 510 Ω

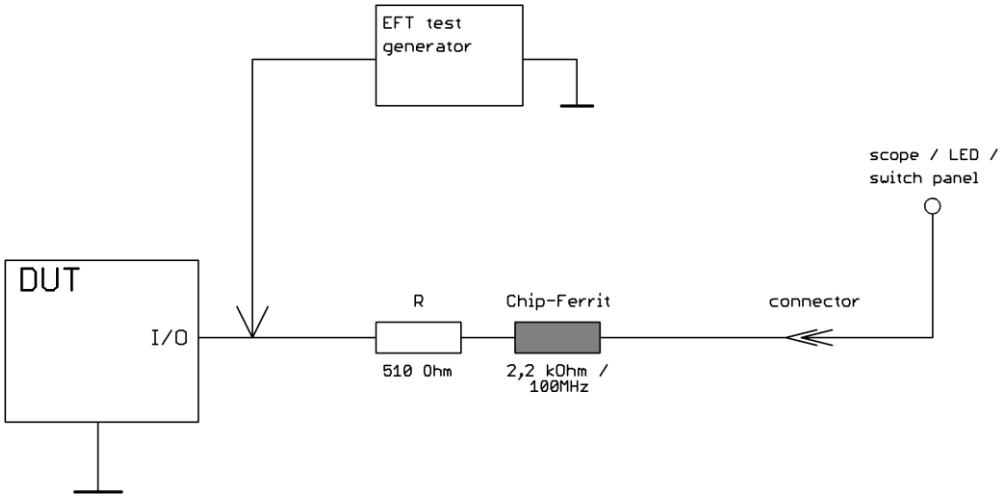


Figure 20 - example of the external set-up on a signal line

EFT test generator on a signal line. Filter elements prevents leading the disturbance.

3.6 Oscillator

- circuit set-up as advised by the manufacturers
- chip-ferrite: approx. 500 Ω at 100 MHz for the relevant oscillator frequency

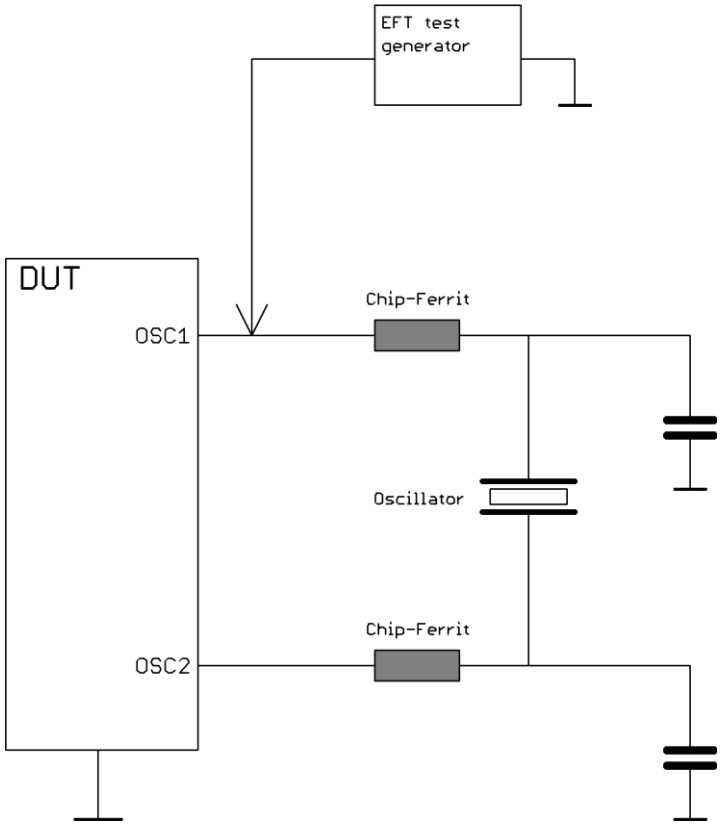


Figure 21 - example of the external set-up on the oscillator pins

3.7 Failure detectors

3.7.1 Failure detector 1 – “Heartbeat LED“

- output pin of the IC with the “Heartbeat LED” signal
- monitored by the Connection Board
- filter: chip-ferrite 2.2 kΩ at 100 MHz or higher
  resistor R ca. 510 Ω

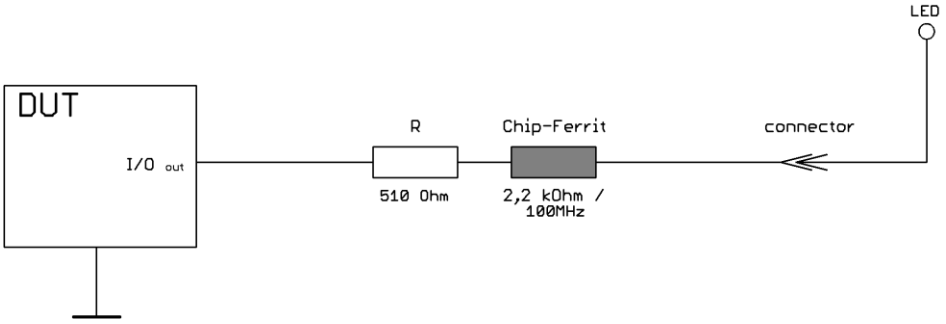


Figure 22 - example of the external set-up on failure detector 1

3.7.2 Failure detector 2 – “Failure LED“

- output pin of the IC with the “Failure LED” signal
- monitored by the Connection Board
- filter: chip-ferrite 2.2 kΩ at 100 MHz or higher
  resistor R ca. 510 Ω

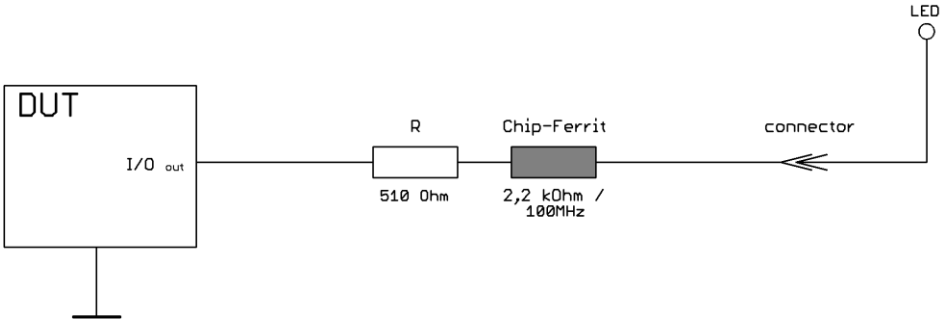


Figure 23 - example of the external set-up on failure detector 2

3.7.3 Failure detector 3 – internal RESET

- circuit as manufacturer advice for user
- operated and monitored by the Connection board
- approx. 47 kΩ pull up resistor (if no internal pull up)
- filter: chip-ferrite 2,2 kΩ at 100 MHz or higher
- resistor R ca. 510 Ω

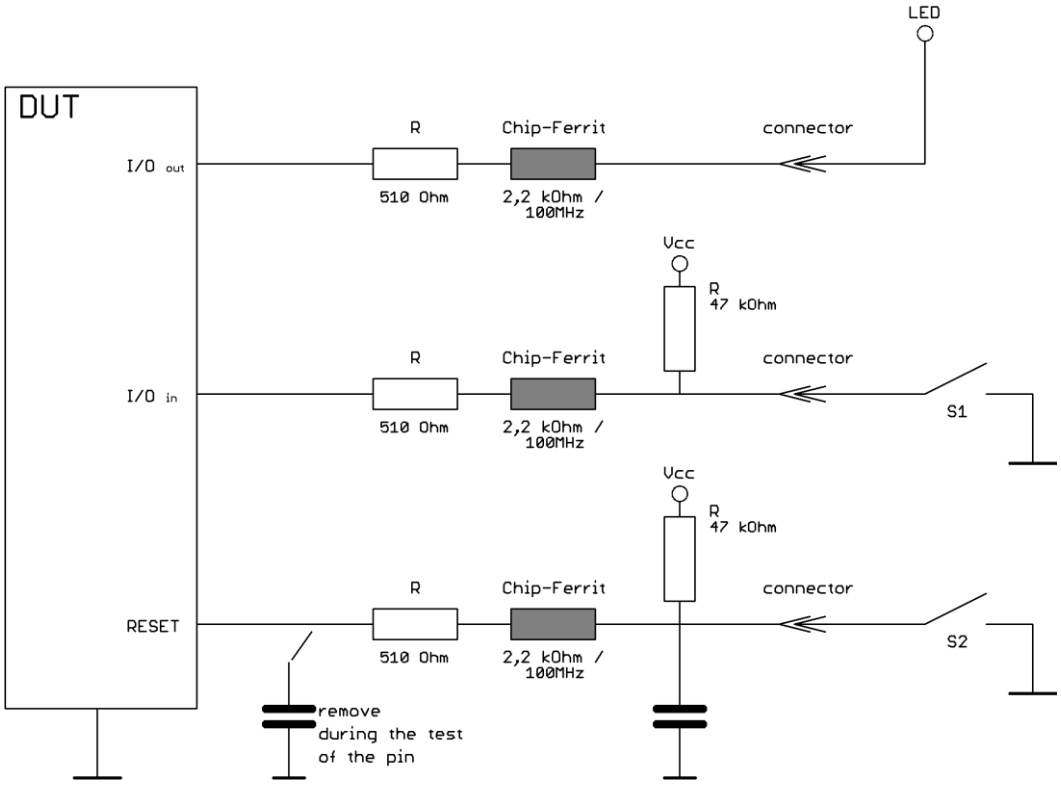


Figure 24 - example of the external set-up on RESET, input and output port

3.7.4 Failure detector 4 – Tristate gathering with scope

- output pin set to high level
- approx. 2.2 kΩ pull down resistor
- filter: chip-ferrite 2,2 kΩ at 100 MHz or higher
- resistor R ca. 510 Ω

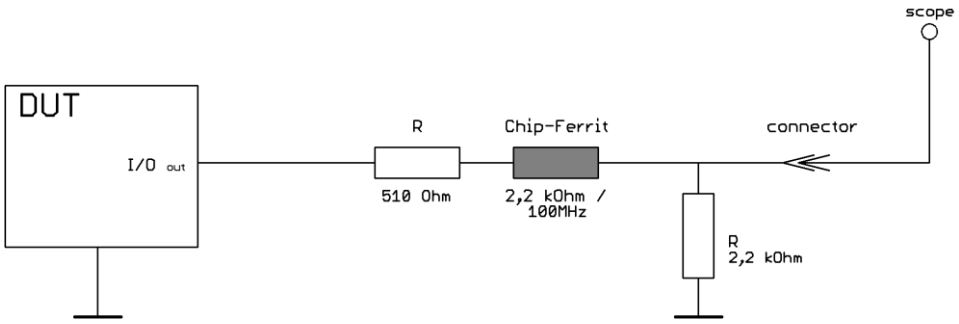


Figure 25 - example of the external set-up on an output pin (for monitoring with scope)

4 TEST STRATEGY

The test set-up should allow the tester to couple test pulses into an IC via conductors.

Definition of representative characteristics:

- Universally valid test results
- Reproducibility
- RF-proof integration of the IC in the test set-up without interactions
- Easy IC exchangeability
- Test of different IC housings / types of pins
- Quick change of the test generator from one pin to the next
- Flexible monitoring

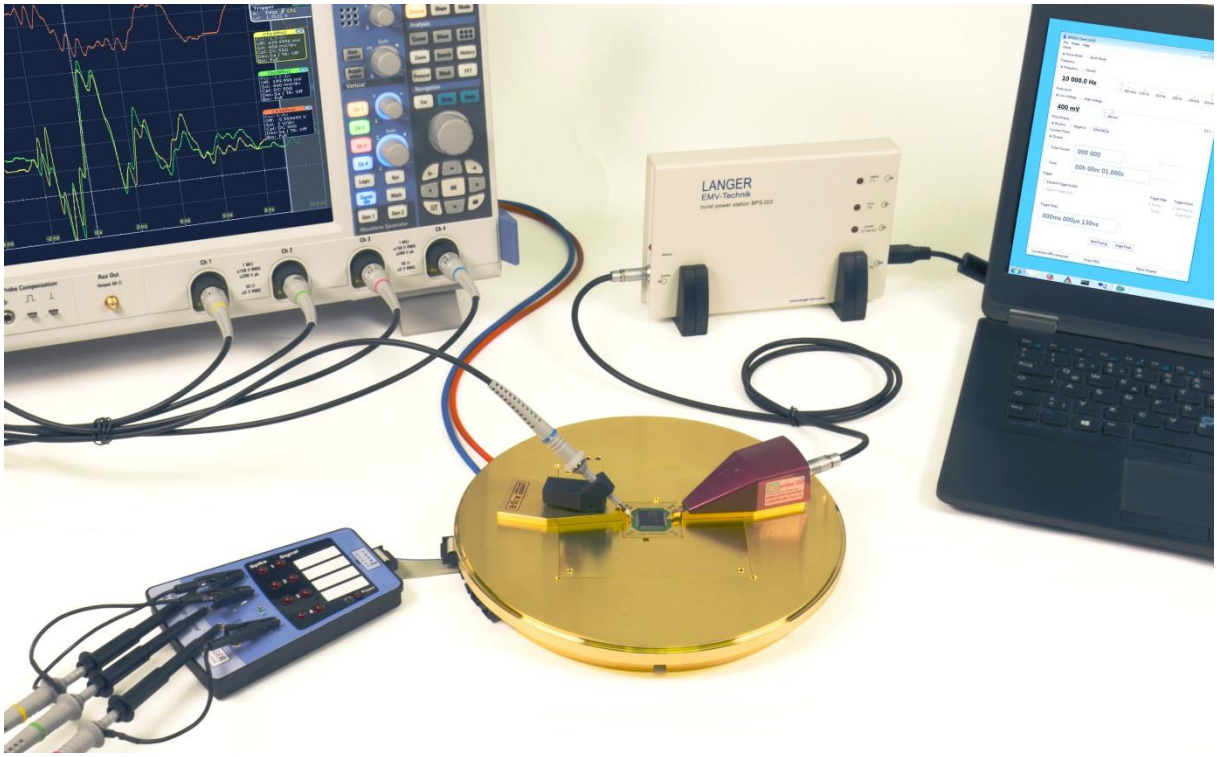


Figure 26 - typical test set-up for pulse immunity

4.1 Test process

Two different test sequences are defined depending on the objective:

1. Qualification test (sequence-controlled voltage rise test)
2. Pre-compliance test (event-driven cause studies)

Qualification test

Definition of:

Test pulse:	P202 → 1.5 / 5 ns P302 → 1.5 / 20 ns
Initial voltage:	Lowest voltage value of the respective probe
Increment of voltage rise:	P202 → approx. 1 V P302 → approx. 10 V
Max. generator voltage:	P202 → 40 V P302 → 500 V
Pulse frequency:	10 kHz
Polarity:	Positive and negative pulses
Pulse duration:	6.55 s → 65500 pulses
Current input of IC:	Manufacturer-dependent Fault if value stays below or is exceeded by 50%
Oscillator:	Use internal oscillator if possible
Fault detectors:	See section 2.4 (software) and 3.6 (hardware)
Display of state "Fault LED":	Software-dependent

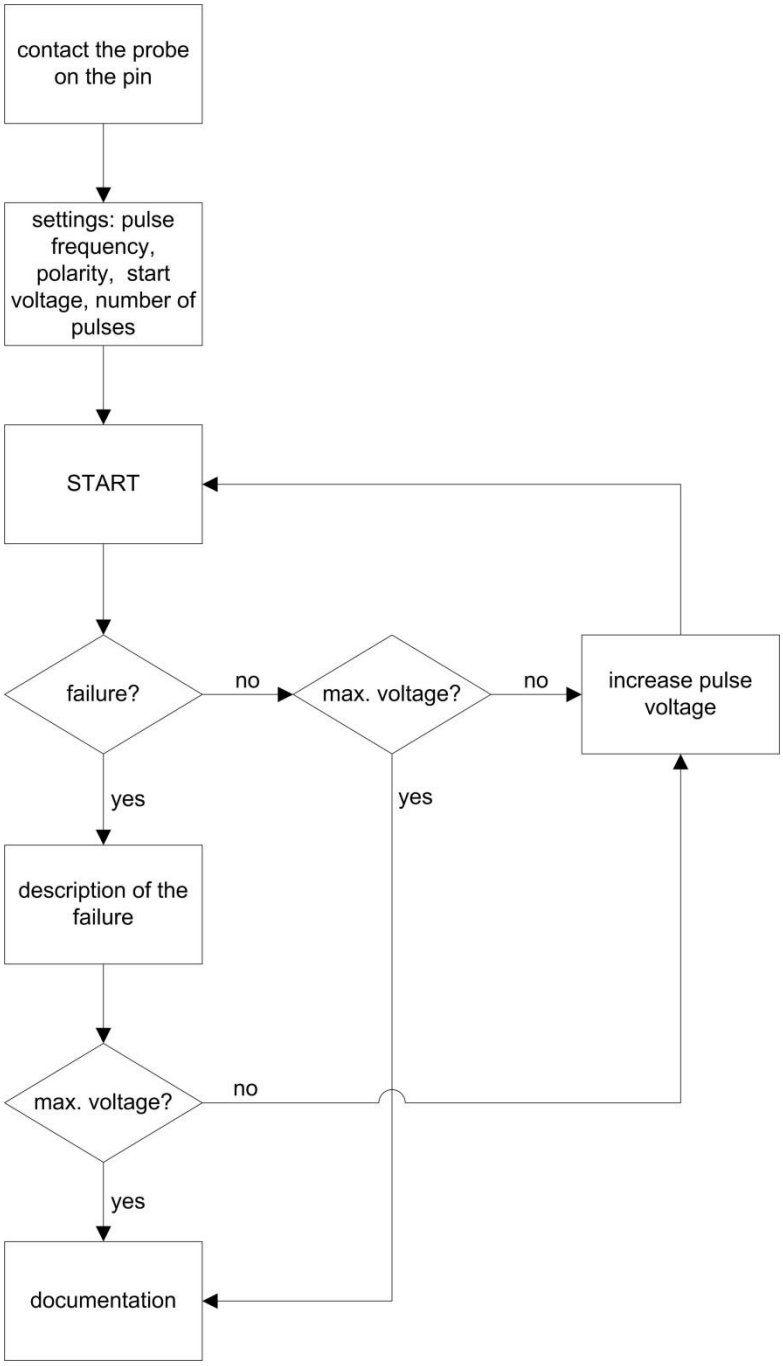


Figure 27 – test procedure for pulse test

Pre-compliance test

The causes of the individual functional faults are studied in this test. In general, these studies are performed during the IC's development phase and with the assistance of the manufacturer's development engineers.

4.2 Fault assessment

Each individual pin is tested up to the highest voltage value of the respective generator. This ensures that all fault patterns are discovered and not concealed. The faults are classified and documented on the basis of the following criteria:

F1.x No interference

F2.x Functional fault where the original functionality is restored automatically at the end of the disturbance coupling

F3.x Functional fault where the original functionality is restored only by a manual RESET at the end of the disturbance coupling

F4.x Functional fault where the original functionality is restored only by a power OFF / ON Reset at the end of the disturbance coupling

F5.x Permanent non-resettable interference with the DUT, e.g. operational failure, increased current input, latch-up, etc.

4.3 Preparation of the test report

The test report should include the following items:

- Circuit diagram of the adapter circuit-board
- Photos of the top and bottom layer of the adapter circuit-board
- Pin-out of DUT
- Software code (as a file attachment) possibly with flowchart
- Detailed fault description
- Overview of test results with P202
- Overview of test results with P302

4.4 Evaluation of immunity

Recommended evaluation of the immunity test results on IC's with pulse probes:

P202 - pulse current injection

Immunity of supply pins:

Voltage at probe (off-load voltage)	**Evaluation of the immunity**
< 3 Volt	very low
3 ... 10 Volt	low
10 ... 20 Volt	medium
> 20 Volt	high

Immunity of signal pins:

Voltage at probe (off-load voltage)	**Evaluation of the immunity**
< 10 Volt	very low
10 ... 20 Volt	low
20 ... 25 Volt	medium
> 25 Volt	high

P302 - pulse voltage test

Immunity of signal pins:

Voltage at probe (off-load voltage)	**Evaluation of the immunity**
< 50 Volt	very low
50 ... 150 Volt	low
150 ... 300 Volt	medium
> 300 Volt	high

Langer
EMV-Technik-GmbH
Noethnitzer Hang 31
DE-01728 Bannewitz
www.langer-emv.com
Tel.: +49(0)351/430093-0
Fax: +49(0)351/430093-22
mail@langer-emv.de