Conducted Impulse Injection Method (CIIM)

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Abstract — **Test methods for electronic systems EUT (Equipment Under Test) are well adapted in the electronic industry. Burst-tests as defined in IEC 61004-4 are well known and electronic systems, devices and apparatus get tested in accordance to above recommendations. In order to get EMS compliance the electronic system has to withstand a certain level of injected EFT-signals. Today the system designer requests EMS-characterisation on IC (VLSI) level in order to be able to predict the final application systems performance. The challenge is now to find a measurement methodology which provides the best possible correlation between IC-device level and final application system level EMS performance. This paper describes a measurement method to analyse the EMS-behavior of ICs.**

1. INTRODUCTION

Conducted Impulse Injection Method (CIIM) describes a measurement method to evaluate the immunity against a single pulse and/or repetitive applied pulses (burst) which get injected into pins of ICs. Depending on the pulse-generator it is possible to inject pulses in either signal pins or power-supply pins of the DUT. The described methodology applies conducted injection to any pin of the DUT (IC, VLSI) in order to evaluate the immunity of the IC against the violating pulse/pulses (EFT-signals). In accordance to the various I/O-characteristics of the VLSI an adequate pulse-generator has to be applied to provide the violating pulse (Electrical Fast Transient - EFT-signal). The necessary test-equipment and the test setup to evaluate the immunity behavior of the DUT gets demonstrated. Finally real measurements on VLSI's have been derived and the results get discussed.

2. OVERVIEW

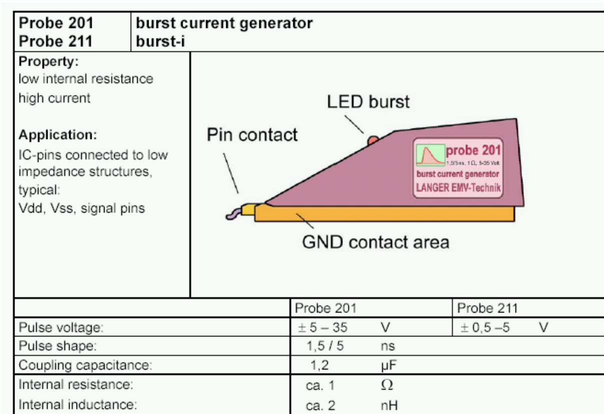
There exist several measurement methods which deal with pulses and how they get injected into the EUT (Equipment Under Test). The main reason to apply these test methods is to analyse the sensitivity (robustness) of an electronic system (EUT) under real environment conditions. As an example, system test in accordance to IEC 61004-4 gets applied to the EUT in order to measure the margin of robustness against EFT-signals applied to a system application. When analysing the measurement results you are not able to isolate the signal path causing the encountered malfunction of the EUT. Of course above mentioned method has been developed in order to detect the margin of sensitivity of an application system (EUT) to indicate only a "go" "nogo" situation. There are no means to detect the signal path which is the rootcause of the detected malfunction of the embedded controller (VLSI) used in this system application. There exists a strong demand on the market to find measurement methods which would allow to correlate the ICs-inherent EMS (Electro Magnetic Susceptibility)-behavior of an embedded controller with the EMS systems (EUT)-behavior. The objective of this paper is to describe a measurement methodology which allows to evaluate the immunity of an IC against injected EFT-signals. The proposed measurement method has to be simple, economical affordable and reliable to allow to measure immunity behavior on chip level. The method applied to the DUT should obtain solid and reproducible measurement results which allow to predict the immunity behaviour of the IC (DUT). Main focus of this immunity measurement methodology is to evaluate the immunity of the IC itself and not the immunity of the surrounding application hardware, the DUT is embedded. Measured results of CIIM provide the system engineer with data about the immunity margin of the IC he(she) intends to use in the system application. Comparison measurements between various IC vendors and/or immunity measurements between different mask-sets, device shrink-levels of the same IC vendor can be made in order to get serious information about the immunity behaviour of the IC. Immunity as well as emission of an IC are device-inherent features which are not documented on today's product data-sheets. Beside the traditional ac/dc, timing parameters and functional descriptions of the various on-chip modules, data about EME (Electro Magnetic Emission) and EMS (Electro Magnetic Susceptibility) are catching increased interest from the system designer. Above mentioned criteria as chip-inherent behavior shows influence to the overall application system EMC (Electro Magnetic Compatibility) behaviour.

3. MEASUREMENT METHODOLOGY

This section describes the measurement technique to evaluate the susceptibility against conducted injection of a single pulse or repetitive pulses (burst-signal) of ICs on chip level. The main difference to the established EFT test method in accordance to IEC 61004-4 is based on the fact that a dedicated puls generator is used and that the coupling of the EFT pulses is different Applying IEC 61004-4 method pulses get coupled either into the supply rails of the system and/or into signal cable harness of the EUT. In contrast the CIIM method couples the EFT pulse or burst signal directly into the pin of the IC (DUT). Characteristics of the injected pulse (burst signal) in the time domain depends on the dedicated pulse generator used. Depending on the various impedance characteristic

of the various I/O structures of the DUT (IC) its necessary to apply a pulse generator which offers the adequate source characteristic to the dedicated pin under test. This differentiation in the characteristics of the used pulse/burst generator allows the user to inject EFT signals to every pin of the DUT. This feature is of importance because under real environmental conditions very often we recognize that dedicated “high impedance”-I/Os (like RST, INT, OSC1, OSC2…pins) on embedded controllers show high sensitivity to coupled noise signals.

The pulse/burst-signal generators are designed to offer different source driving impedance characteristics. The two different equivalent circuits of these pulse/burst generators are optimized in their source impedance and serial signal coupling capacity .Series 3xx contains Probe 301, Probe 311 with their 100 Ohm/18pF. Pulse/burst generators of the 3xx series will be used to inject EFT signals into I/Os which show high impedance characteristics, I/Os which are not designed to drive heavy loads (Fig 1).



	Probe 201		Probe 211	
Pulse voltage:	± 5 – 35	V	± 0,5 –5	V
Pulse shape:	1,5 / 5	ns		
Coupling capacitance:	1,2	µF		
Internal resistance:	ca. 1	Ω		
Internal inductance:	ca. 2	nH		

Fig. 1 Probe 2xx series, probe characteristics

Pulse/burst generators of the 2xx series (Probe 201, Probe 211) are used to inject EFT signals into I/Os which show low impedance characteristics, I/Os which are designed to drive heavy loads (Series 2xx consists of Probe 201, Probe 211 with their 1 Ohm/1,2µF)

Provisions on the CIIM test system are made to synchronize the pulse/burst signal with a trigger signal provided by the DUT. This feature enables the user to evaluate the DUT immunity behaviour from a “time variant” point of view, in contrast to the usual applied method to evaluate the immunity behavior of the DUT from the “time invariant” point of view.

One of the key issues of the pulse/burst signal to be injected into the pin of the DUT is the “shape” of this EFT pulse. The question arises which is a proper shape of the pulse to be injected?. In order to provoke any functional failure (i. e. inverter with P- and N-channel MOS transistor) of the DUT it’s necessary to apply a pulse with a certain amplitude, rise-time, duration and fall-time. In other words the pulse (EFT signal) must show a certain “voltage over time integral” in order to be able to switch the inverter, but not to destroy its circuitry.

Amplitude must be higher than the threshold of this inverter and pulse duration has to be longer than the inverters inherent signal propagation delay. These conditions have to be met to provoke the switch-event at the internal stages of the IC. As result of this investigation we defined pulses to be injected into the pin of any DUT(IC) which have to be positioned in the region where the “static noise level” changes to the “dynamic noise level”. This region of “dynamic noise immunity level” depends on technology and topology implemented on the chip (DUT) to be tested. Fig 2 shows an example of graphs which represent the “static” as well as the transition region to the “dynamic” noise threshold. As complexity and speed of VLSIs increase in more or less continuous way from year to year we can recognize the shift of this threshold to shorter times. On the very left position of this graphs you could imagine the “Dirac-Impulse” with infinitely short pulse duration and infinitely high amplitude.

Signals with their shape in the time domain positioned left of the graph cannot cause any switching-event at the inverters stage of the DUT. Simulations and practical evaluations of today’s state of the art VLSIs (µC, DSPs, Hybrid µC…) have shown have shown that impulse (EFT) – signals with rise times in the range of 1ns and pulse durations of aro some ns force an inverter (buffer) to switch. The pulse amplitude has to be higher than the threshold voltage of this inverter. Above data is based on embedded µC with 0,25µm HCMOS technology used in many various applications (industrial-,automotive-,consumer- market segments).

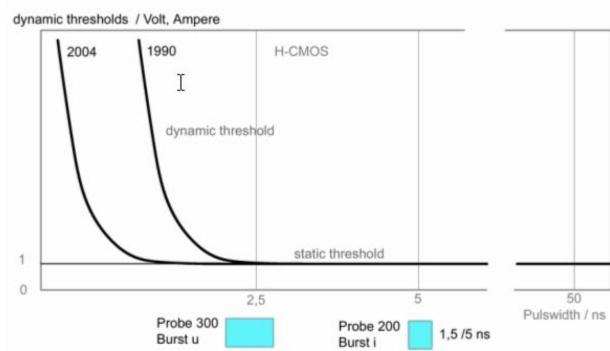


Fig. 2 general graph to demonstrate “static” – and “dynamic” – threshold on HCMOS technology

Another key-issue raises the question n about the real requirements of the pulse generator. What range of voltage amplitudes do we need for pulses to inject into the various pin characteristics of the DUT?. Too much energy of the applied pulse could irreversible damage the semiconductor internal structure. What has to be the proper internal source impedance of the pulse/burst generator? In order to get a clear picture of all these

variables we have to generalize the features of the various pin characteristics the DUT offers.

4. DUT PIN ANALYSIS

Power supply pins:
In general, power supply pins offer low impedance and therefore the pulse generator injecting pulses into these pins has to offer low impedance. The real true pulse shape injected into these pins can develop in the chip-internal structure and provoke the intended switching effect in the DUT.

Bi-directional pins:
If a bi-directional I/O or an unidirectional output is switched to static “high” or “low” level, this pin also offers a low impedance to the generator.
Bi-directional I/O pins which carry dynamic signals like clock-signals, PWM-signals, address-data-signals..etc. may offer high or low impedance to the pulse generator.

Pins utilized for dedicated functions:
Pins like RES, INT, IRQ, BKGD, OSC1, EXTAL… on µC offer high impedance to the applied pulse generator.

As result of above categorized pin-impedance characteristics the various pins of the DUT make it necessary to use two different types of pulse generators to provide the EFT signal to the pin . These requirements reflect the availability of two different impulse/burst generators, Probe 2xx-series with Probe 201 and Probe 211 (Fig 3) and probe 3xx-series containing Probe 301 and Probe 311 (Fig 4).

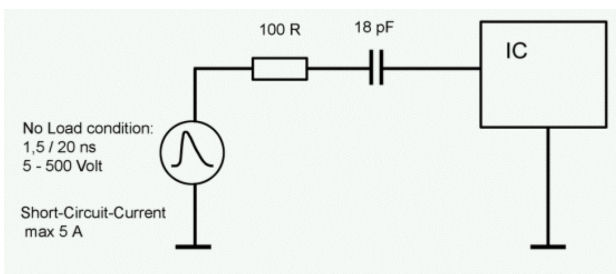


Fig. 3 Simplified equivalent circuitry of Probe 2xx series pulse/burst generator

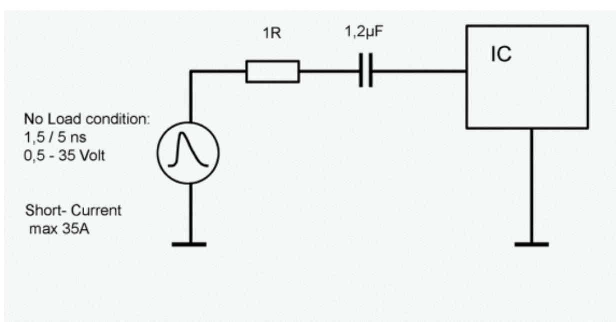


Fig. 4 Simplified equivalent circuitry of Probe 3xx series Pulse/burst generator

Fig. 5 and Fig. 6 demonstrate the “shape” of the EFT signal under various load conditions

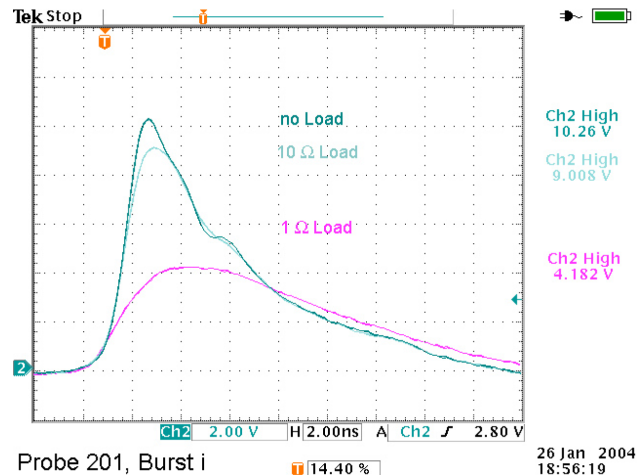


Fig. 5 Pulse generator Probe 201, EFT voltage shape under various load conditions

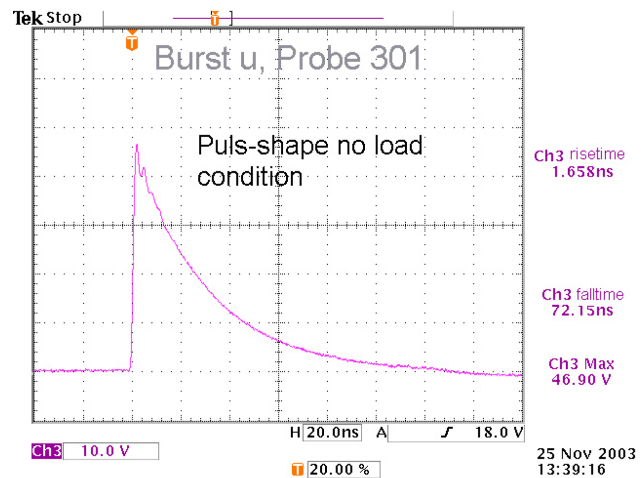


Fig. 6 Pulse generator Probe 301 voltage shape without any load

Two different pulse/burst generators are necessary to ensure serious analysis on the behaviour of the DUT when EFT signals are injected into the pins of a µC (DUT). The CIIM measurement method ensures further that the DUT can operate in its regular mode whereas EFT signals can be injected in every pin. It depends on the dedicated test software program which internal functional modul of the microcontroller is operating and simultaneously gets violated by injected pulse/burst signals. The higher the effort in test softwareprogram the more reliable the result which will indicate malfunctions and anomalities in functionality of internal on-chip integrated sub.modules. Test program philosophy occupies an important part of the measured result. You will have to ensure that the chip-internal communication

path doesn't get disrupted during your dedicated chip-internal functional modul test. Intelligence has to be applied on how to trace and monitor on-chip functionality during EFT signal violation of the DUT. How do you get reliable information about functionality out of the victim (DUT) and how you can monitor it outside the device?

5 EXPERIMENTAL MEASUREMENT / TEST SETUP

Block diagram of the test setup of the Conducted Impulse Injection Method (CIIM) is illustrated in Fig 7.

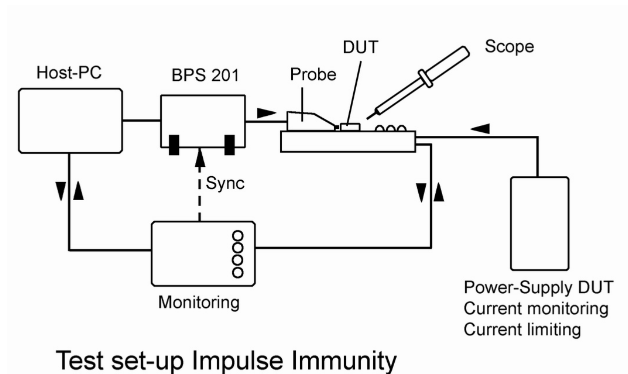


Fig. 7 CIIM block diagram of test setup

Measurement can be done either with control of the host PC or in offline stand alone mode.
The DUT (IC, VLSI) is soldered on a small multilayer EMS testboard (Fig. 8, Fig. 9). In order to carry the variety of the many different available IC packages, three EMS testboard sizes have been predefined. As an example the 64 pin QFP package of a midrange controller is assembled on the EMS testboard with 22,7mm x 22,7mm 4-layer PCB.

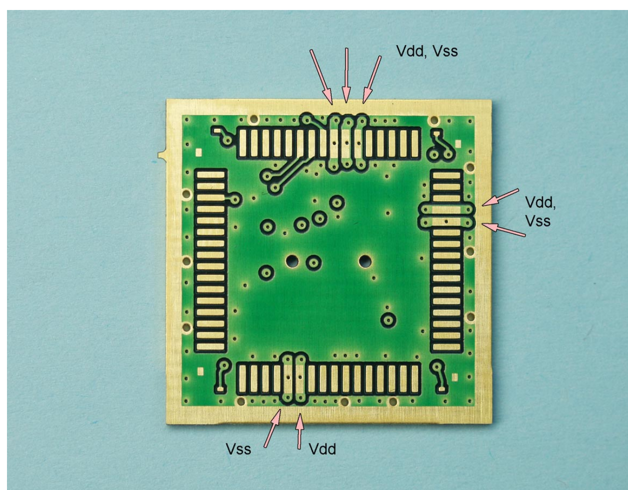


Fig. 8 EMS testboard 4-layer unassembled, top side with dimensions 22,7mm x 22,7mm for 64 QFP DUT (µC).

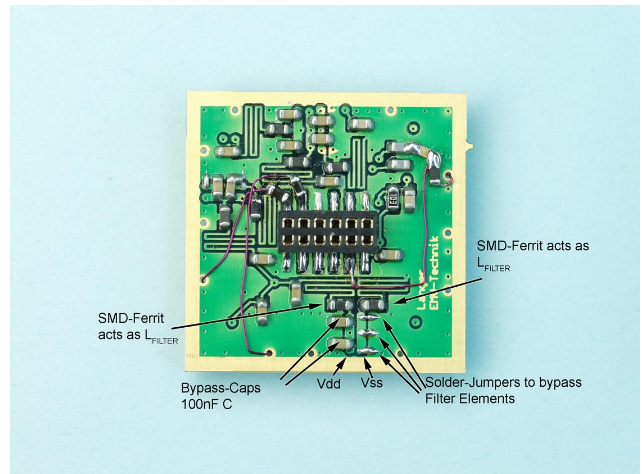


Fig. 9 EMS testboard assembled, bottom side

This EMS testboard is embedded in a massive groun-plane (Fig. 10).
There exists exact coplanarity between the slide surface of the Probe 2xx/3xx (Pulse generator) ond the top sode of the EMS testboard in order to minimize the current loop-back area and therefore minimize the total loop inductance of the measurement setup.

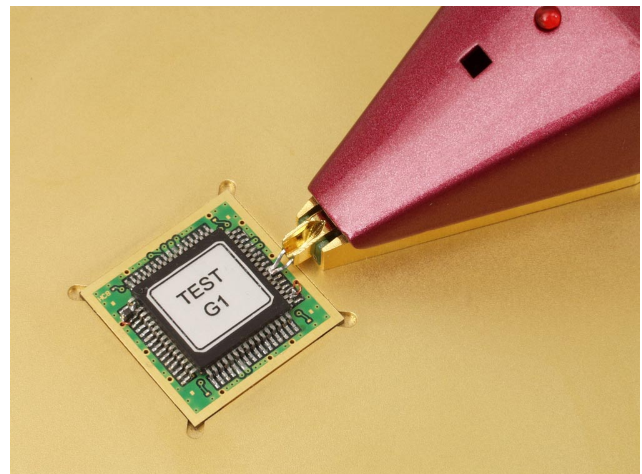


Fig. 10 DUT 64 QFP µC assembled on EMS testboard with Probe tip connected to pin

The DUT gets supplied by an external power supply which should be equipped with current monitoring and electronic dhort circuit protection. Probe 2xx or Probe 3xx contains the pulse/burst signal generator. The probe gets supplied with power and control signals by BPS201 station modul. Provisions are available to monitor the status of the DUT (Monitoring LEDs may be used in an external monitor modul or the LEDs may be assembled on the EMS testboard to indicate the status of the DUT. It's also possible to communicate the failure status of the DUT via the onchip SCI or SPI interface to the host PC, if the applied test program supports this function on the

DUT. Additionally signals of the DUT can be measured by means of an oscilloscope probe as indicated.

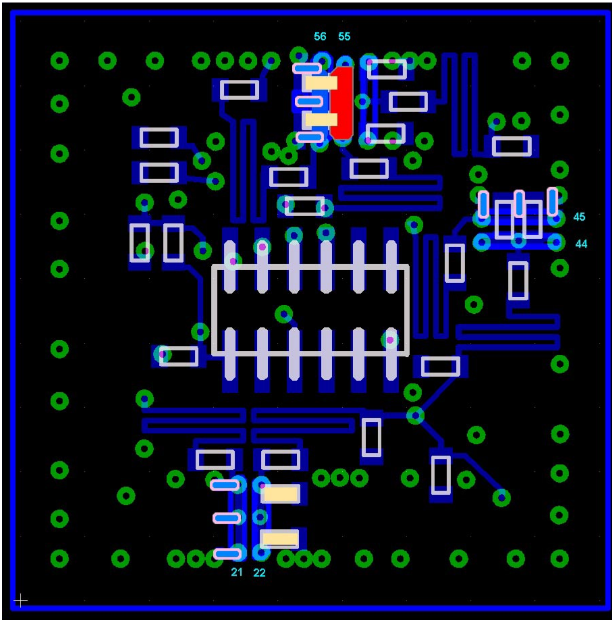


Fig. 11 Pin preparation on bottom side of EMS testboard to define EFT signal injection path (Bypass caps, SMD ferrite filters, solder jumpers)

Depending on the pin category where the pulse/burst signal will be injected, provisions have to be made on the bottom side of the EMS testboard to arrange th desired injection path on the DUT by adding/removing bypass capacitors, filters solder jumpers (Fig. 11)

Fig. 12 Simplified equivalent circuitry of DUT (HCMOS – IC) with possible EFT signal injection points.

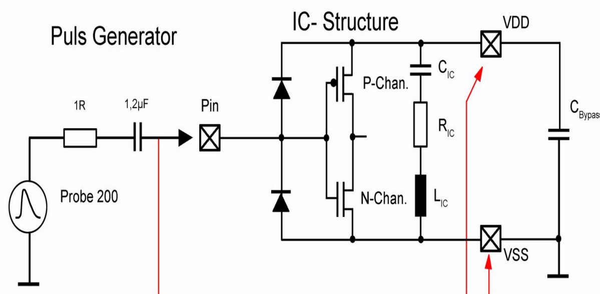


Fig. 12 reflects a simplified IC equivalent circuitry and shows how the pulse/burst generator can be applied to the various pins (pin categories) of the DUT. The current flow of the injected EFT signal can be analysed in the circuit. If a positive EFT signal is injected into the input pin of the victim, the corresponding current flows through the upper inherent input protection diode towards the positive supply rail and via bypass capacitor back to the signal source. If a negative pulse is applied to the input pin current flows from VSS through the diode towards the input pin back to the pulse generator. EFT signals can also be injected to the VDD and VSS and output pin of the DUT. In order to be sure that the EFT signal shape (time domain) the Pulse generator provides also developes at the tested pin of the victim its important that the generators source impedance and coupling capacitor meets the requirements of the load impedance where the EFT signal gets injected. Pulse/burst generators of series Probe 2xx/3xx fulfil these requirements. In order to have more flexibility concerning the adjustment of Pulse amplitudes the probes P201 and Probe 211 differ in the adjustable pulse amplitude. Both versions provide positive as well as negative pulse/burst signals. Probe 201 is optimized for EFT signal amplitudes in the range +/-5V …+/-35V, whereas Probe 211 provides amplitudes in the low voltage range +/-0,5V…+/-5V. Similar differentiation is offered in the probe series 3xx,. Probe 301 provides +/- 120V…+/- 500V, Probe 311 provides +/- 5V…+/-140V.

6 CONCLUSION

This paper demonstrates a new conducted impulse immunity measurement method which allows the user to inject EFT signals into every pin of the DUT during regular operation.
Practcal exercised measurements have shown and convinced that measurement results obtained with this method are reproducible and focus on the inherent EMS behaviour of the DUT when violated with EFT signals.
The applied method enables the user to perform reliable susceptibility data of an IC (VLSI). The methodology concentrates on the EMS of the "silicon die" and the package because the setupof the test fixtureminimizes the impact of external environment. As example the whole real application of a 64 QFP µC runs on the EMS testboard with dimensions which are about the same as the footprint of the DUt occupies. The EFt signal to be applied to the dedicated pin of the DUt is positioned as close as physically possible and ensures a low impedance high frequency signal current path. The dynamic current caused by the applied pulse generator flows in a very low inductive signal path. Its amplitude is defined mainly by the impedance of the impulse generator and the pin related impedance of the victim.
Experimental results carried out by the proposed method can be used twofold:
First the chip designer can used the derived analysis data for EMS improvements in future designs (redesigns) and second the system designer can use these data for predictions how his system EMS behaviour might be if he embeds the characterized IC in his system.