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Dimensional design of connectors in terms of EMC immunity to burst and ESD

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1 Objective

How should connectors be designed to manage disturbances that are coupled in such as burst and ESD? How can the disturbance immunity of connectors be specified? Which mechanisms of action does the interference follow? Interface systems such as USB, LVDS, Ethernet, CAN, as well as real-time systems derived from these and internal device signal connections such as data / address bus systems, etc. have a certain resistance to interference.
Connectors are the weak points in the signal chains. This paper describes the EMC characteristics needed by a connector to resist interference.

There is one EMC parameter which can be assigned to every connector, namely the coupling inductance. This is a universal constant whose value only depends on the connector's metal structure. This constant can be determined for each type of connector.
Due to their different switching thresholds, interference thresholds and protective measures, the various data transmission systems also have different demands on the value of this constant.
Effective EMC design is only possible if both the inductance factors which fulfil these demands and the inductance factors of the connectors in question are known.
A corresponding data collection [1] has to be built up and consistently supplemented over a longer period as a basis for the implementation of this approach in practice. The data collection must also contain representative disturbance values which the different types of disturbance generators can provide to ensure universal use.
These correlations are described by taking an LVDS system as an example.

2 Mechanisms of action

Interference with interface systems is mainly via the connectors. This is based on clear physical mechanisms of action which describe the interference process and which can be used to draw conclusions about the electromagnetically compatible design of connectors. Unfortunately, today's design principles are not based on these mechanisms of action. The present state of technology is thus characterized by connectors with a poor disturbance immunity and poor disturbance emissions characteristics. In the past, redundant electronic systems were used to compensate these disturbance immunity shortcomings. The requirements on speed and safety, however, have risen so that connectors of a better EMC quality are required.

Interference with signal leads in the connector is based on Faraday's law (1).

$$u_{ind} = d\Phi / dt = L \, di_{Disturb} / dt \qquad \textbf{(1)}$$

The magnetic flux Φ which passes between the ground (screen) contacts and the signal pin induces the voltage u_{ind} in the signal pin. The flux Φ is generated by the disturbance current $i_{Disturb}$ coming from the cable sheath and flows through the ground contacts of the connector. The inductance L is the decisive parameter for the connector's EMC quality. The denser the design of the ground contact system, the smaller the inductance L and the voltage u_{ind} that is induced in the signal pins. The aim is to keep the inductance small enough that the induced voltage remains below the signal interference threshold. The inductance is zero if the connector has a completely closed and consistent metal sheath. The inductance values of electronic connectors are in the range from 1 pH to 10 nH and closely connected with the design of the connector's metal structure.

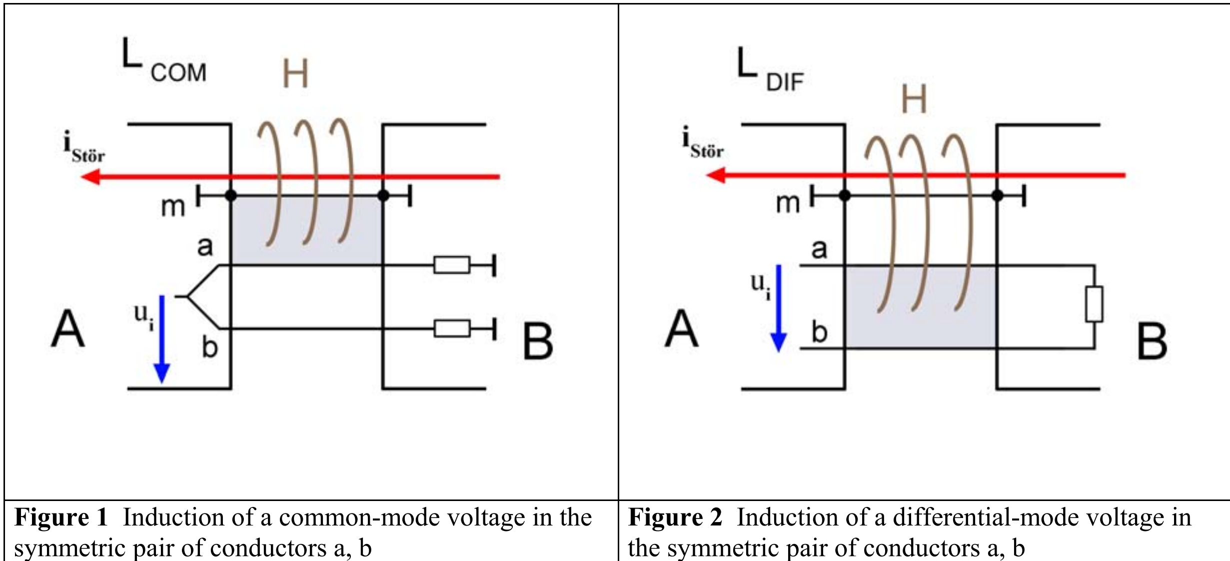

Figure 1 Induction of a common-mode voltage in the symmetric pair of conductors a, b

Figure 2 Induction of a differential-mode voltage in the symmetric pair of conductors a, b

There are two voltage induction possibilities for symmetric pairs of conductors (**Figure 1, Figure 2**, a, b). A common-mode voltage **Figure 1, Figure 3** and equation (2), is induced in both signal pins a and b if the magnetic field H passes between the two of them and the ground contact m. A differential-mode voltage **Figure 2, Figure 4** and equation (3), is induced between the two signal pins a and b if the magnetic field H passes between them.

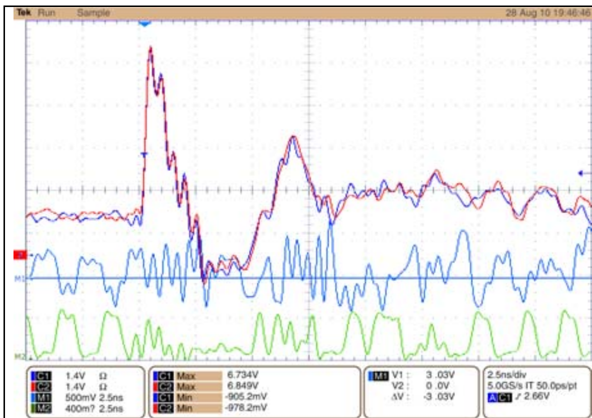

Figure 3 1 Gbit LVDS system, common-mode disturbance coupling via a connector at L_{COM} = 1 nH. The current of a 2 kV ESD pulse induces the voltage u_{COM} = C1, C2.

Difference signals = C1, C2; M1 = C2-C1; M2 = LVDS receiver out.

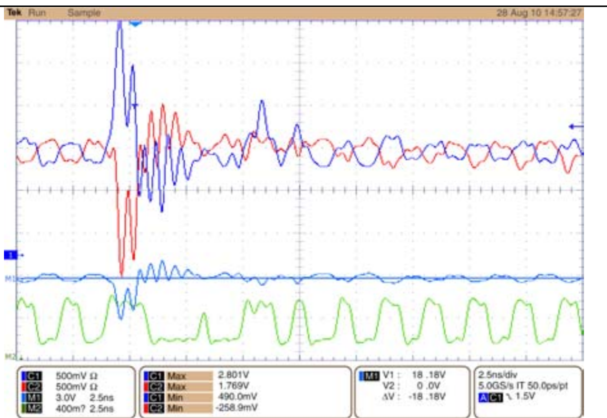

Figure 4 1 Gbit LVDS system, differential-mode disturbance coupling via a connector at L_{DIF} = 2 nH. The current of a 0.5 kV ESD pulse induces the voltage u_{DIF} = M1 = C2-C1.

Difference signals = C1, C2; M1 = C2-C1; M2 = LVDS receiver out.

$$u_{ind} = u_{COM} = d\Phi_{COM} /dt = L_{COM}\, di_{Disturb} /dt \qquad (2)$$

$$u_{ind} = u_{DIF} = d\Phi_{DIF} /dt = L_{DIF}\, di_{Disturb} /dt \qquad (3)$$

The inductances L_{COM} and L_{DIF} induce the voltage in the connector. Both inductance values are a constant quantity for each type of connector which is directly connected to its structural design. The disturbance generator's share in voltage induction depends on its di / dt.

3 Disturbance generator effect

Burst and ESD disturbance pulses have different interference effects. A parameter has to be created for the interference effect to allow a universal description of the interference.

The interference effect parameter of a disturbance generator is its maximum di / dt. According to Faraday's law (1, 2, 3), di / dt causes the interference in the connector. The maximum is reached in the area of the disturbance pulse's front edge at an ideal generator short-circuit. The generator current increases to $\hat{I} = \hat{U}_{Gen} / R_{Gen}$ over the rise time T_A. Hence it follows that:

$$\mathbf{(di / dt) = \hat{U}_{Gen} / (R_{Gen} \; T_A)} \qquad \mathbf{(4)}$$

(di / dt) is proportional to the generator voltage $\hat{U}_{Gen}$. Division by the generator voltage results in the interference effect k_{GEN} :

$$\mathbf{(di_{Disturb} / dt) / \; \hat{U}_{Gen} = 1 / (R_{Gen} \; T_A) = k_{GEN}} \qquad \mathbf{(5)}$$

$$\mathbf{\hat{U}_{ind} = L \; k_{GEN} \; \hat{U}_{Gen}} \qquad \mathbf{(6)}$$

The constant k_{GEN} is the measure of the interference effect of a disturbance generator. The measured k_{GEN} values differ from the calculated values. ESD generators have higher values which are mainly caused by internal stray effects. The values are smaller for burst generators due to an unfavourable L/R relationship of the disturbance current circuit. Maximum k_{GEN} values can be measured for practical applications, whereby the type of generator must be taken into account in this connection. Information required for practical applications can be retrieved from data collections [1]. Values are given in Table 1.

Generator type	R_{Gen} [Ω]	T_A [ns]	k_{GEN} [A/ns kV] from $1 / R_{Gen} \; T_A$	k_{GEN} [A/ns kV] from measured di / dt	Delta
Burst	50	5	4	1.4	-75%
ESD	330	1	3	3.5	+15%

Table 1 Calculated and measured k_{GEN} values. Conditions for the measured values: The ESD pistol was placed directly on the metal surface. The burst generator had an external line current path with a length of 50 cm.

Apart from the desired pulse shape, ESD generators may generate high-frequency transients in the range between 2 and 3 GHz [2]. These transients decay after a few ns. Only very fast IC can be influenced by such phenomena (core voltages of 1 V, structural widths <100 nm). The LVDS receiver acts like a low pass (**Figure 5** and **Figure 6**). It can only follow the 1 ns event and thus operates the "LVDS out". The faster 2.2 GHz event causes no change in the logic state of "LVDS out" which means that k_{GEN} Table 1 is valid. This ESD generator provides a value which is about twice as high (k_{GEN} approx. 7 A/ns kV) for more sensitive IC. Devices with such ICs may react more sensitively.

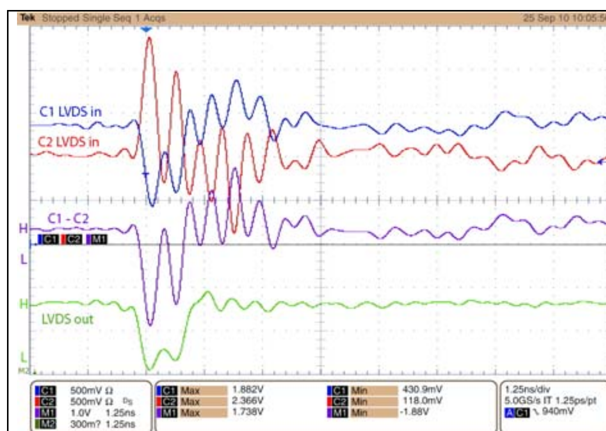

Figure 5 Effect of a 0.2 kV ESD pulse that is directly coupled into the receiver connector on the LVDS-IC in the signal state H

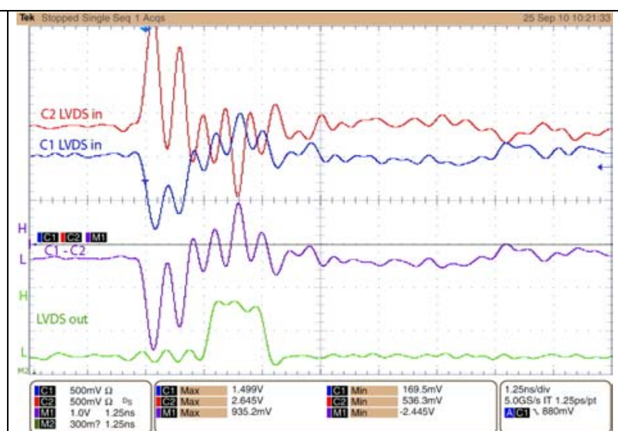

Figure 6 Effect of a 0.2 kV ESD pulse that is directly coupled into the receiver connector on the LVDS-IC in the signal state L

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4 Disturbance coupling effect in a symmetric conductor system taking LVDS as an example

L_{DIF} and L_{COM} couple different voltages into the LVDS system. These voltages encounter two different signal interference thresholds:

Differential-mode voltage $\mathbf{u_{DIF}}$:	Switching threshold	$U_{Threshold}$	= 360 mV
Common-mode voltage $\mathbf{u_{COM}}$:	Clipping voltage of the clipping diode	U_{Diode}	= 2.5 ... 5 V

The differential-mode disturbance signal **Figure 4** is superimposed on the 1 Gbit differential-mode useful signal (C1, C2). The differential voltage is shown in channel M1 = C2-C1. Bit errors are produced if the coupled in differential voltage reduces the LVDS signals by 360 mV (M1 = 0 V). The corrupted data stream is noticeable on the (M2) output of the LVDS receiver.
The disturbance threshold is much higher with common-mode disturbances **Figure 3**. The disturbance signal must reach the switching voltage of the clipping diodes. The diodes then short circuit the data signals so that no more data can be received. Burst produces a differential voltage of almost zero (**Figure 11**). The high-frequency transients produced by the ESD pistol are dominant in ESD.
Adaptation is lost as soon as the clipping diodes become conductive. Reflexions develop which repeat bit errors periodically after the transit time.
The interference threshold relationship between DIF and COM is around 1:10.

5 Bit error-free data transmission systems

No disturbance voltages which could generate bit errors may be allowed to enter data transfer systems if these are to be free from bit errors. Consequently, the connectors' coupling inductance must be small enough that the disturbance current from the disturbance generator only induces a voltage which is lower than the data lines' interference threshold.

$$\hat{U}_{ind} = \hat{U}_{DIF} < U_{Threshold} = 360\text{ mV} \quad (7)$$
$$\hat{U}_{ind} = \hat{U}_{COM} < U_{Diode} = 2.5 \ldots 5\text{ V}$$

These systems can be data / address bus systems or special real-time systems.
The required inductance values can be calculated on the basis of the signal interference threshold $U_{Threshold}$ of the data system, the generator voltage $\hat{U}_{gen}$ to be withstood and the interference effect k_{GEN} of the generator (worst case).

It follows from (6) that:

$$L = U_{Threshold} / (k_{GEN}\, \hat{U}_{Gen}) \quad (8)$$

Figure 7 and **Figure 8** show the equation (8) for a LVDS system which is subjected to burst and ESD. According to the planned disturbance immunity (ESD and burst in kV), the appropriate connector can be selected on the basis of its coupling inductance in the run-up to electronic development. It is assumed that the coupling inductance values are known for the connectors in question [1].
This also applies to internal data lines without error protection which are mostly individual lines led via board-to-board connectors inside the device. The interference threshold corresponds to the switching threshold of the logic family [3] that is used.

RJ45 connector system	$\mathbf{L_{DIF}}$ **[pH]**	$\mathbf{L_{COM}}$ **[pH]**
Socket	10 ... 100	400 ... 800
Plug with cable shield	5 ... 500	50 ... 4000
Plug contacts	0.8 ... 30	50 ... 200

Table 2 Range of coupling inductance values measured for RJ45 connector systems, last revised 2010

The ranges of inductance values for RJ45 connector systems in **Table 2** and the correlation to the generator voltage **Figure 7** and **Figure 8** show that RJ45 plug contacts are able to withstand ESD-CD voltages in the range of 7 ...> 30 kV via the differential-mode coupling path and voltages in the range of 14 ...>30 kV via the common-mode coupling path. The sockets are considerably poorer. Depending on the respective type, cable plugs may already be interfered with by bursts of $\leq$ 0.2 kV but they can also withstand bursts of > 8 kV. The burst example shows that reliability today depends on the random choice of type. RJ45 connector systems are particularly critical if data transfer is without error protection.

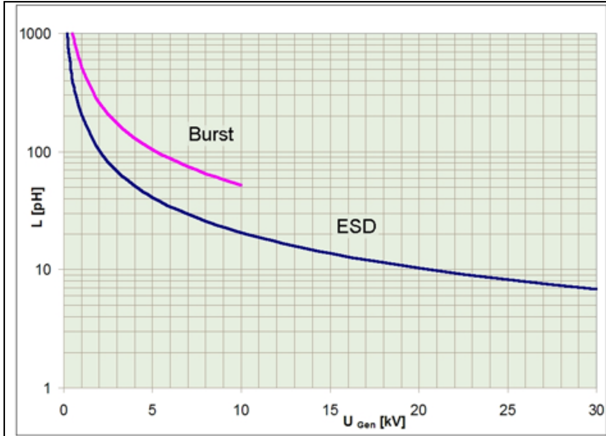

Figure 7 Permissible inductance L_{DIF} of a connector as a function of the test generator voltage for a signal threshold of 360 mV, where k_{GEN} 1.4 A/ns kV and 3.5 A/ns kV

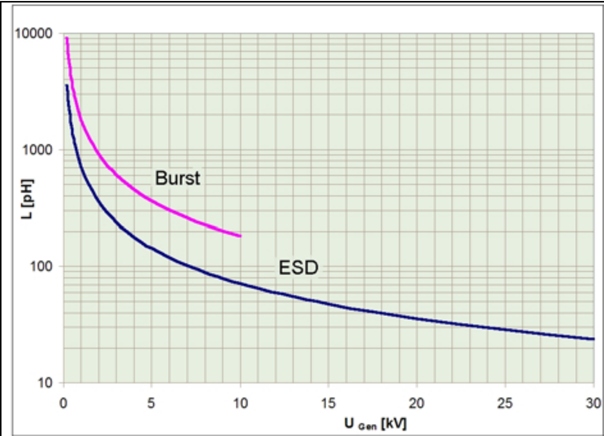

Figure 8 Permissible inductance L_{COM} of a connector as a function of the test generator voltage for a signal threshold (clipping voltage of the clipping diodes) of 2.5 V, where k_{GEN} 1.4 A/ns kV and 3.5 A/ns kV

	Burst: 2 kV, where k_{GEN} 1.4 A/ns kV	ESD CD: 6 kV, where k_{GEN} 3.5 A/ns kV
L_{DIF} [pH], threshold: 360mV	260	35
L_{COM} [pH], threshold: 2.5V	900	120

Table 3: Coupling inductance limit values taken from **Figure 7** and **Figure 8** for burst of 2 kV and ESD CD of 6 kV

The values in **Table 3** are the maximum total inductance values of the connector system for the bit error limit. They are valid without a reserve factor. In general the reserve factor is >1.2. The target for safe systems is a reserve factor of 10.
The correlations for RF injection can be derived from (1) and (6).

$$U_{Threshold} = I_{Disturb} \ \omega \ L \ / \sqrt{2}$$

The equation is valid for the RF peak current $I_{Disturb}$ range. **Figure 9** shows the maximum permissible currents calculated for some inductance values. The bigger the interference current, the more severe the bit corruption. The RF current can be injected according to the BCI method in practice.

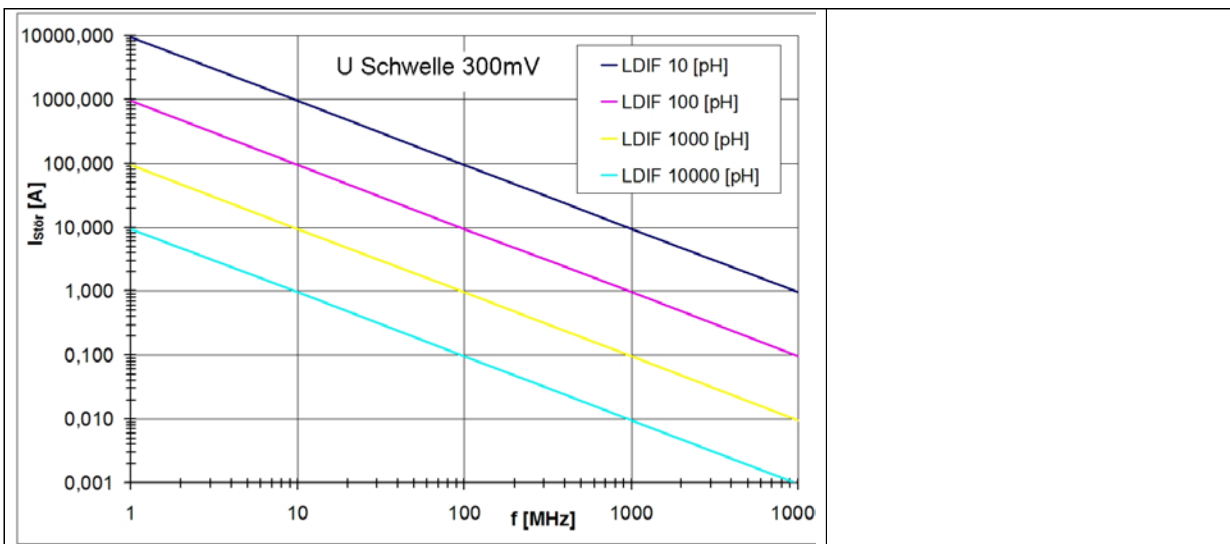

Figure 9 Limit values calculated for RF injection into connectors

6 Influence of error protection

There are different strategies to prevent or detect and correct bit errors. These strategies build on each other.

1. Multiple sampling of a data bit and majority decision (filter)

2. Bit error detection and correction, only a limited number of bits can be corrected.

3. Repetition of messages (re-send) if the number of correctable bits is exceeded.

4. Re-setup of link

It may not be possible to sufficiently implement multiple sampling for very fast systems and repeating messages may not be allowed for real-time systems. Real-time systems without repetition are the real bottle-neck. Only a limited number of erroneous bits can be corrected in this case. The mechanism of disturbance injection is such that the number of corrupted adjacent bits increases as a function of the disturbance's rising peak value. As of a certain number of corrupted adjacent bits, the error protection measures taken are no longer useful.

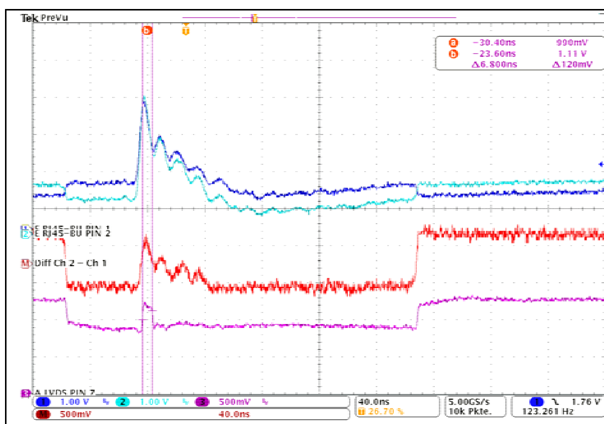

Figure 10 Response of a LVDS system to a 1 kV burst injection into a CAT 5E cable plug.
C3: output of the LVDS receiver.
Bit corruption: 6.8 ns, bit width of 250 ns

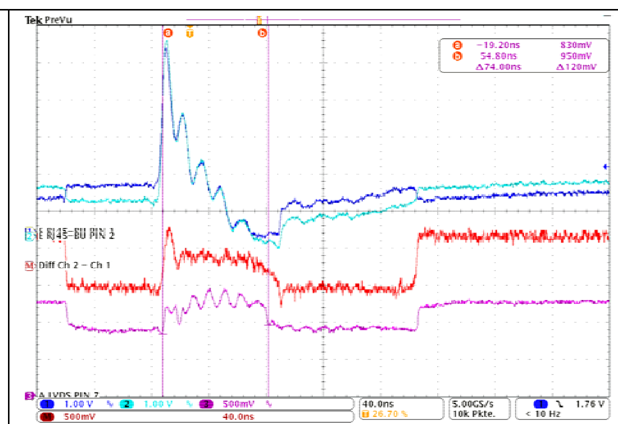

Figure 11 Response of a LVDS system to a 1.5 kV burst injection into a CAT 5E cable plug.
C3: output of the LVDS receiver.
Bit corruption: 74 ns, bit width of 250 ns

The figures **Figure 10** and **Figure 11** show the effect a burst pulse on a CAT 5 E cable plug for a LVDS system. It can clearly be seen that the common-mode share is of primary importance. The common-mode share, however, has a higher interference threshold (clipping diodes) and does not become effective in **Figure 10**, the differential-mode share is responsible for the interference in this case. The common-mode share also exceeds the interference threshold in **Figure 11**. The voltage on the signal lines exceeds the clipping voltage of the clipping diodes in the event of interference (**Figure 11**). The diodes become conductive and short-circuit the data signals. The bit corruption time increases with the peak value of the disturbance voltage **Table 4**. The higher the data rate, the smaller the bit width and the more bits are corrupted. 7 bits would be corrupted in a 100 Mbit system (bit width of 10 ns) if the interference **Figure 11** interferes with data transfer for 74 ns.

$\hat{U}_{Gen}$ [kV]	T_Z [ns]
1	6.8
1.5	74

Table 4 Bit corruption T_Z at burst on a CAT 5E cable plug

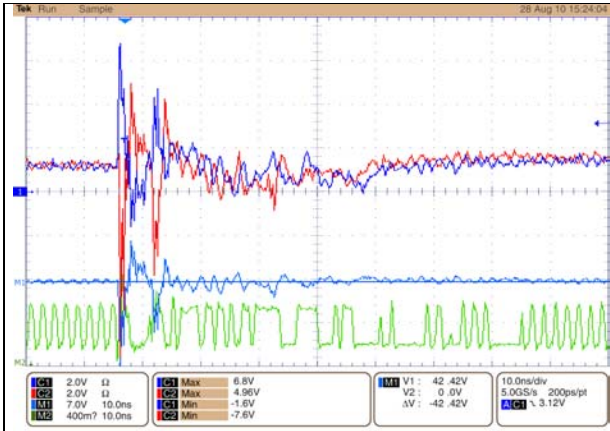

Figure 12 Response of a 1 Gbit LVDS system to 5 kV ESD CD injection via a differential-mode inductance of 2 nH.
M1 differential signal C2-C1, M2: output of the LVDS receiver.
Bit corruption: around 70 ns

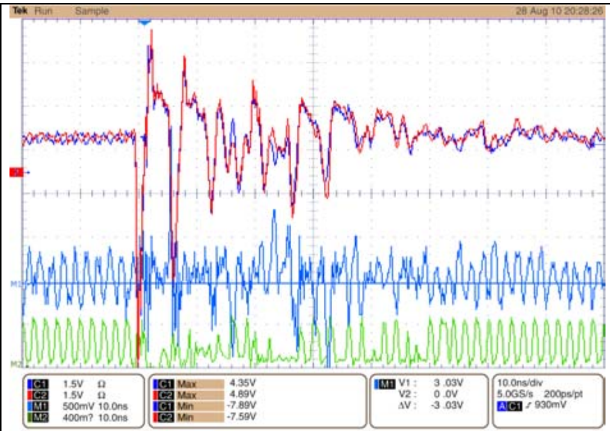

Figure 13 Response of a 1 Gbit LVDS system to 8 kV ESD CD injection via a common-mode inductance of 1 nH.
M1 differential signal C2-C1, M2: output of the LVDS receiver.
Bit corruption: around 50 ns

Under the influence of an ESD injection, the pulse form, clipping diodes and reflexion phenomena worsen the bit corruption **Figure 12** and **Figure 13**. The number of corrupted adjacent bits also depends on the peak value of the generator voltage **Figure 14**. The number of corrupted adjacent bits leaps ahead as soon as the clipping diodes become effective (**Figure 14** generator voltage between 0.5 and 1 kV).

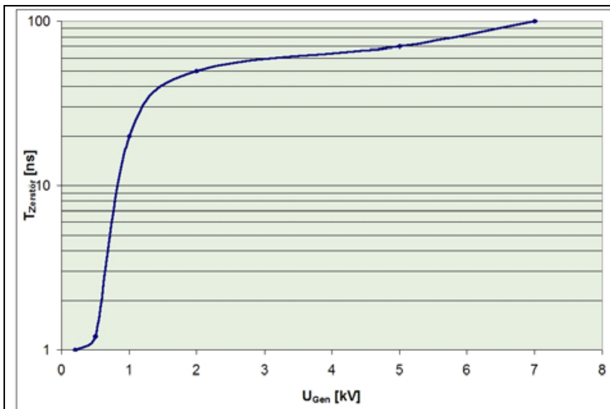

Figure 14 Number of corrupted adjacent bits for a LVDS system as a function of the ESD generator voltage at a connector differential-mode inductance of 2 nH.

The number of corrupted adjacent bits is the limiting factor for both reliable multiple sampling and error correction. The issue can be solved by a respective low coupling inductance of the connector systems **Figure 7** and **Figure 8**.
It is important to know how many adjacent bits are corrupted for system dimensioning. Guide values for the number of corrupted adjacent bits can be recorded in data collections depending on the parameters (L_{DIF}, L_{COM}, etc.).

7 IC function interference thresholds

Apart from the IC signal interference thresholds, IC function interference thresholds may also be of significance [4]. Malfunctions will occur in the IC as soon as this threshold is reached. Its level is generally above that of the signal interference thresholds. The value depends on the IC type and can be a voltage induced between 1 and 500 V. These function interference thresholds normally become effective via the IC's internal clipping diodes.

They allow the disturbance current to penetrate deeper into the IC. Depending on the respective complexity, it can cause diverse malfunctions. In the simplest case the malfunctions can cause additional data transfer errors. Total failure may be the consequence in the worst case. Any error is possible even the most inconceivable. The relevant errors can only be determined by experiments and are classified according to their severity [4]. The error thresholds can be recorded by common-mode and differential-mode interference. A data collection then comprises:
- IC signal interference thresholds
- IC function interference thresholds
including potential malfunctions and conditions of use

8 Summary

The previous sections described how disturbances are coupled into electronic systems via connectors taking an LVDS interface as an example. In practice attempts are made to combine LVDS and RJ45 connector systems. RJ45 connector systems have been developed for Ethernet. In this connection the effect of their relatively high common-mode inductance is blocked by magnetic couplers. Systems without magnetic couplers will respond more sensitively. This approach can also be applied to simple data lines (D/A bus, etc.) which are led via board-to-board connectors. Before the disturbance current can penetrate these connectors, it is attenuated while passing through the device. This can be taken into account by a device factor [3]. A worst case assessment can be made if no device factor is available. The coupling inductance of a board-to-board connector depends on its ground and signal assignment [3].
This paper should help electronics developers develop sturdy devices. In future, connector users will be able to choose a connector which is ideal for their needs in terms of EMC on the basis of the coupling inductance. Connector developers can design connectors for special purposes. A prerequisite for this approach is that the coupling inductance to be achieved must be known for the respective area of application.
Increasing demands for safe and fast electronic systems will speed up this development.

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