

Characterizing the Immunity of Integrated Circuits against Electrical Fast Transient Disturbances

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***Abstract** – The constant growth of microelectronic components in our modern electronic systems makes great demands on the electromagnetic compatibility (EMC) of the integrated circuits (ICs). To determine the electromagnetic compatibility of ICs the IEC (International Electrotechnical Commission) is just working on two new standards to characterize their electromagnetic emission and their susceptibility. Unfortunately, the current version of the susceptibility standard does not include measurement methods to characterize the susceptibility of ICs to electrical fast transient disturbances. In this paper a new measurement method, which was developed especially for this kind of characterization is introduced.*

1 Introduction

During the last years the operating frequencies as well as the integration density of ICs have increased significantly. On the other hand the supply voltage levels as well as the channel length of IC has decreased. Therefore engineers have to deal with higher electromagnetic emissions and lower immunities to electromagnetic interferences of their developments. As the susceptibility of a final product might only depend on just one single IC, the characterization of the EMC at the IC level is getting more important. A lot of electronic system designers therefore ask for electromagnetic emission measurements and susceptibility tests of the ICs they are going to use in their application.

With IC level EMC measurement results from standardized measurement procedures a system designer will be able to estimate the EMC behavior of his product and figure out if it will satisfy the necessary EMC requirements. For this reason, efforts have started years ago to define standardizes measurement methods for the EMC characterization of ICs.

The work group 9 of the IEC subcommittee 47A is currently working on two new standards (IEC 61967 and IEC 62132) for the characterization of the electromagnetic emission and the immunity of ICs. These two standards provide the semiconductor manufacturers

and their customers defined measurement methods, which can be used as a basis for the characterization.

To test the immunity of ICs, the IEC 62132 describes several measurement methods. At present only the immunity against amplitude modulated and continuous wave radio frequency signals is suggested. The susceptibility against transient disturbances, such as fast transients (bursts) is currently not included in this standard. As testing against transient disturbances is a very important part in the immunity characterization, a measurement method like the one which will be introduced in this paper should also be implemented for IC testing.

2 Fast transient immunity test at system-level

Over the past 20 years testing the immunity against fast transient disturbances (bursts) is an inherent part of the susceptibility characterization of electric and electronic devices. The first standard (the IEC 801-4) on this topic was published in 1984. Later, this standard was changed without technical modifications to IEC 1000-4-4. Since 1995 the standard circulates under IEC 61000-4-4 [2].

The IEC 61000-4-4 defines immunity requirements and test methods for electrical and electronic equipment to repetitive electrical fast transients such as those originating from switching transients (interruption of inductive loads, relay contact bounce...). The standard also defines the test voltage waveform, the range of the test levels as well as the test equipment and setup for coupling transients into power supply, control and signal ports of electrical and electronic equipment.

Figure 1 shows a general graph of these fast transients. The waveshape of a single test pulse has a rise time of about 5ns and an impulse duration of 50ns (50% value). The repetition period of this single pulse depends on the test voltage level and is indicated in table 1. The burst duration is defined with 15ms and repeats every 300ms. The duration of the test should be not less than 1 minute and both (pos. and neg.) polarities have to be tested.

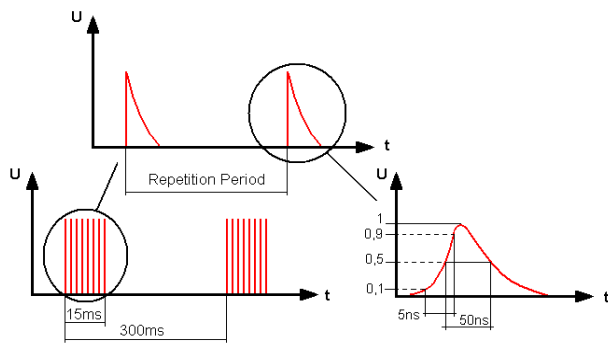


Figure 1: General graph of fast transients.

In table 1 the test levels for testing power supply ports and for testing I/O signal, data, and control ports are given. The test levels should be selected in accordance with installation and environmental conditions.

Open Circuit output voltage and repetition rate				
Level	Power supply		I/O ports	
	kV	kHz	kV	kHz
1	0,5	5	0,25	5
2	1	5	0,5	5
3	2	5	1	5
4	4	2,5	2	5
X	special	special	special	special

Table 1: Test levels.

A coupling clamp is used to couple the fast transients/bursts to the device under test (DUT). Two kind of coupling devices are used. For coupling to the power supply port a so-called coupling/decoupling network is used. A capacitive coupling clamp is used to couple the transients to I/O interfaces of communication, data, and control ports. The coupling capacitance of the clamp depends on the diameter, the material, and the shielding of the cable. Its typical value ranges from 50pF to 200pF. The isolation between the DUT and a metallic ground reference plane shall be 0.1m. The ground plane shall be at least 1x1m and project beyond the DUT by at least 0.1m on all sides. The length of the connector between the EFT generator and the clamp should not be longer than 1m.

3 A new Burst test system for the IC-level

Up to now there was no measurement system for the IC level available to perform reactionless fast transient testing of ICs. To close this gap a measurement system that satisfies all the requirements at the IC level was developed by Langer EMV-Technik GmbH.

To design a burst generator for the IC level, all the corresponding characteristics of an IC, as well as the voltage level which actually occurs at the IC pin have to be considered. A decisive prerequisite for a correct measurement is the right connection to the IC (DUT). Therefore a reference plane (a massive GND plane) is

used in which the DUT is placed via a chip adapter board (see figure 2).

Depending on the kind of measurement, different burst generators (probes) can be used. These probes are placed on the reference plane and are electrically connected to it. A pin contact is used to couple the bursts into the IC pin. This measuring setup, especially the usage of a reference plane, guarantees that correct measurements up to the GHz range can be performed.

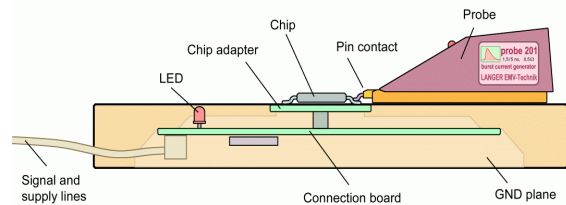


Figure 2: Schematic measurement setup.

In order to perform burst measurements at the chip level, a chip adapter board has to be fabricated first. This adapter board is then connected to a connection board, which is used to supply the IC and bring it into an adequate operation mode. During the measurement the probe is attached securely to the reference plane by a magnet. This guarantees an excellent ground connection of the probe. The pin of the IC under test, which should be tested, is connected to the probe via the pin contact. The massive GND plane and the small setup allows to measure the operating condition of the IC with an oscilloscope during a burst interference without influencing the measurement results.

3.1 The measurement setup of the Burst test system

To couple burst signals into the IC under test, several burst probes of the series 200 (current injection) and 300 (voltage injection) are available. These probes are supplied by a Burst Power Station BPS 201 (see figure 3). A serial interface to a PC is used to control the probes and to set different burst parameters.



Figure 3: Burst measurement setup with IC under test, test board, probe 201 and burst power station.

4 How do disturbances couple into the IC under test

4.1 Magnetic coupling

Disturbing currents, which can be caused by burst pulses, are flowing on PCB traces and causes magnetic fields B_{St} . This magnetic fields than couple into loops on the PCB and induce noise voltages u_{St} (figure 4). The function of an IC can be interfered in two ways by the magnetic field:

- The induced voltage u_{St} influences the input of the IC. The input circuit can not separate a normal input signal from a noise signal and the IC may consider a noise signal as a logical signal.
- The induced voltage drives a noise current i_{St} into the IC pin. If the IC pin is a VDD/VSS-pin, the noise current is flowing directly to the internal VDD/VSS-system of the IC. It can penetrate however also via an input pin for example trough internal drivers, the protection diodes, or chip inherent stray/parasitic capacitors to the internal VDD/VSS-system of the IC. The VDD/VSS system leads the noise current to further functional parts of the ICs, so that interferences can occur in areas having no direct relation to the interfered pin.

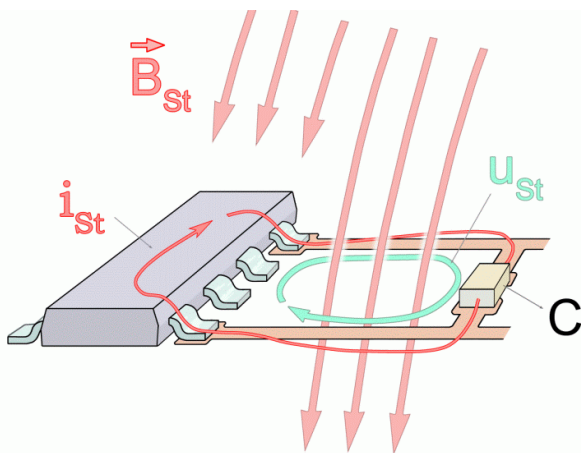


Figure 4: Interference of an IC trough H-field coupling.

4.2 Electric Coupling

The electric fields caused by burst interferences can be up to 10.000V/m. As a burst pulse has a very short rise time with high du/dt an electronic system can be effected by capacitive coupling. In this case a current is generated due to the stray capacitances. Figure 5 shows how electric fields couples into PCBs. Again, there are two ways how the function of an IC can be interfered:

- On the PCB and insight the IC might be resistors to VDD and to VSS. In figure 5 these resistors have been summarized by one resistor R. The

current generates a voltage drop u_{St} across this resistor. The voltage drop is interpreted by the IC as a logic signal and causes a malfunction.

- The current is divided into two parts. A first part flows via the resistor and eventually via an external decoupling capacitor outside of the IC, the second part of the current flows directly into the IC. Protection diodes for example might give a path for the current to flow to several further functional parts and cause similar effects as with magnetic coupling.

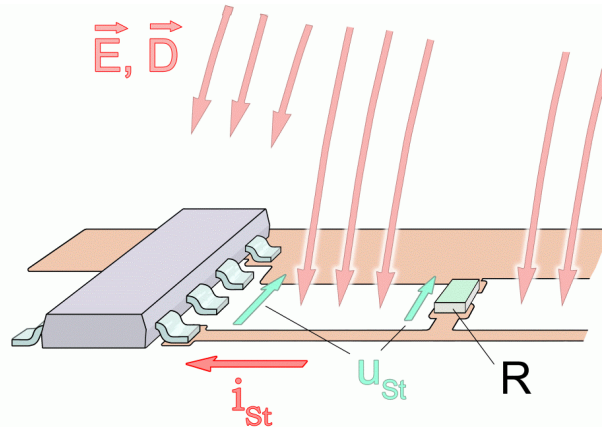


Figure 5: Interference of an IC trough E-field coupling.

5 Burst generators for IC-level tests (conducted coupling)

In addition to the described coupling mechanisms two burst probes are available for coupling burst pulses into an IC.

5.1 Burst probes for magnetic coupling

Probes for magnetic coupling have to recreate the induction loops of the PCB. In the worst case this induction loop can only exist of the internal current path of the IC and the path via the decoupling capacitor connected to the IC pins. In this case the parameters R and L of the current loop can be characterized by the parameters of the IC, which are for the Vdd/Vss pins about 10-100mOhm and 10nH. To keep the probes free from reactions their R and L value was set to be about 10 times smaller. For these measurements, probes of the series 200 are available (see figure 6).



Figure 6: Probe 201 for burst injection.

These probes have a high coupling capacitance (800nF) and offer a very low impedance (about 10 Ω internal resistance and 2nH internal inductivity). The amplitude of the burst pulse can be varied from 3-37V. Figure 7 shows a burst pulse, which has been coupled by a Probe 201 into the Vdd supply pin of an IC.

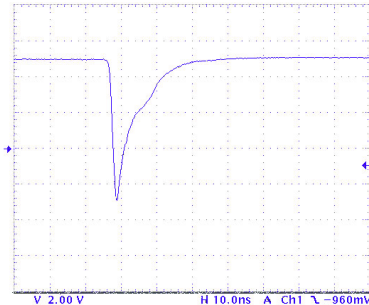


Figure 7: Burst pulse on the Vdd supply.

5.2 Burst probes for electric coupling

Probes from the 300 series have been designed for electric coupling. The probes inject voltage pulses at a rise time of 1ns via a low coupling capacitance (<30pF).

6 Measurement results

One of the main difficulties in doing interference measurements, is to figure out how an interference can be recognized. Sometimes suitable test software to visualize interferences, like for example the switching of certain registers or memory values or the start of an internal RESET, has to be developed before an IC can be evaluated. In the following example the susceptibility of a simple microcontroller was evaluated with the probe 201. The microcontroller was programmed that one of the output ports inverts its value at the end of a program loop. The pulse sequence was monitored during the test with an oscilloscope. Different failures were obtained by injecting burst pulses into the power supply pins of the microcontroller, like the one's listed in table 2.

Pin	severity level	Failure
Vdda	10,4V pos.	Latch up - The controller stops, current input clearly increases -> Danger of destruction.
	2,7V neg.	Controller crashes and restarts automatically. The duty cycle of the timing pattern output on the port is disturbed (Abb. 8)
Vssa	4,0V pos.	RESET triggered. Duty cycle not disturbed.
	10,5V neg.	Controller crashes and starts again by itself. Duty cycle not disturbed.
Vdd	9,6V pos.	Controller crashes and does not start again by itself. Duty cycle disturbed.
	8,0V neg.	Controller crashes and does not start again by itself.
Vss	9,8V pos.	RESET triggered. Duty cycle not disturbed.
	3,6V neg.	RESET triggered. Duty cycle not disturbed.

Table 2: Different failures of a microcontroller

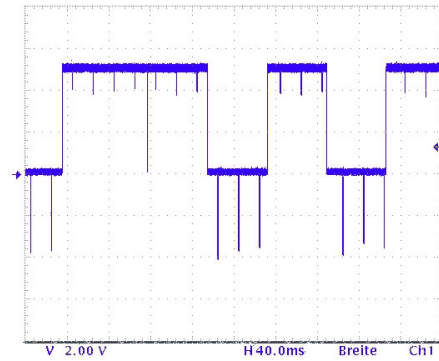


Figure 8: Failure in the duty cycle of the timing pattern.

Many other failures can occur alongside those shown. With the knowledge of the type of coupling (polarity of the burst voltage, function and location of the interfered IC pin) and the failure that occurred, the chip designer can recognize the influence mechanism and is given hints which area of the IC has to be redesigned.

7 Conclusion

Testing the immunity of ICs according to the IEC 62132 standard just characterizes the susceptibility against RF signals. There are no regulations available to test an IC against transient disturbances like bursts. The IEC WG9 SC47A is currently working on measurement methodologies for immunity tests for ICs violating the DUT with ESD signals (bursts). The characterization of electronic devices and systems is regulated since a long time by the IEC 61000-4-4 standard, which is presented briefly. For the characterization of the immunity of ICs against fast transient disturbances, a new burst test system is introduced. The ways how burst interferences can couple into IC pins are shown together with the results, which were obtained by the characterization of a microcontroller.

References

- [1] IEC 62132-1, "Integrated circuits - Measurement of electromagnetic immunity, 150kHz to 1GHz - Part 1: General and definitions", 47A/618/CD,
- [2] IEC 61000-4-4, "Electromagnetic compatibility (EMC) - Part 4: Electrical fast transient/burst immunity test", 1995/01