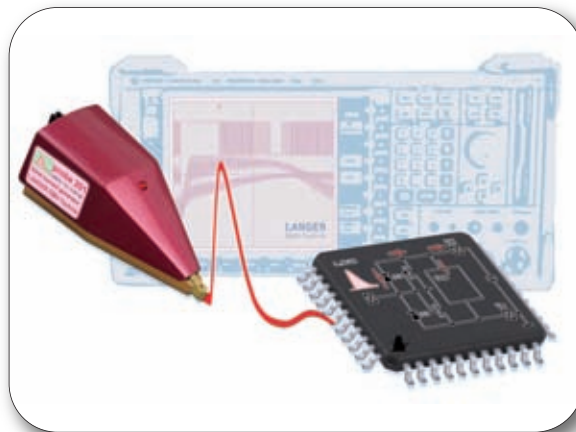


EMC at chip level: assessing IC immunity to pulse disturbances

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Given identical functionality, good EMC characteristics in a product give an IC manufacturer the edge over competitors. The parameters decisive for disturbance immunity need to be determined, allowing engineers to draw conclusions for chip design. Naturally, different IC types need to be compared under the conditions prevailing in the applications.



■ Apart from its layout and housing design, the characteristics of the ICs which are used in a device are decisive for its EMC characteristics. The IC susceptibility to fast pulse disturbances (ESD, burst) increases significantly if their structural dimensions, operating voltages and operating points are reduced. Current developments in the ASIC and micro-controller field tend to structures below 100nm, with even 45nm being reached for computer chip sets. In combination with higher switching rates this results in a drop in disturbance immunity by around 90 percent compared to earlier ICs. This tendency is also reflected by the EMC behaviour of devices.

While standards have been available at the device level for years, there are no such regulations for device parts such as assemblies and components. Increasing complexity, and in particular increasing component integration density, make it more and more difficult to comply with the standards specified for the devices without standardized requirements at the IC level. The IEC 62132 standard describes methods for measuring the immunity of integrated circuits to conducted disturbances. But this standard presently contains only test and measuring methods for continuous and amplitude-modulated RF signals. There is as yet no assessment of immunity to transient disturbances.

The IC test pulses are defined on the basis of the device test procedures. The respective test set-ups generate electric and magnetic fields in the device. These quantities also have a local effect on the interface of the IC package. IC test generators must provide a universally applicable simulation of the disturbances from these electric and magnetic components. Figure 1 shows a typical ESD test set-up. The ESD generator test pulse $u_G(t)$ which is applied to the device under test (DUT) generates a current pulse $i(t)$ that flows through the device. A voltage drop occurs in the device and results in the electric field strength $E(t)$. The current $i(t)$ generates the pulse magnetic field $H(t)$ in the device. These fields have an indirect effect on the IC via the conductor runs connected from outside or any peripherals and, in addition, they also have a direct effect on the IC packages.

It is nowadays normal to indicate the ESD immunity of electronic components in the test specification as a value of one to several kilovolts with reference to the human body model, for example. A 100pF capacitor which is charged to the test voltage is discharged to the DUT via 1500 ohms for this purpose. The test is only used to ensure a certain stability of the IC to destruction when handling the component during manufacture, packaging, transport and assembly. The test object is never in oper-

ation during this test. A differentiation has to be made between the objective of the present directive and that pursued by the test system from Langer EMV-Technik. The ESD immunities specified according to the human body model are not related to the ESD behaviour in operation. The protective mechanisms which are designed for the human body model (without taking into account any disturbances in operation) may even cause problems in functional disturbance tests.

The IC test system from Langer EMV-Technik refers to the ESD and burst immunity of PCBs and electronic devices (IEC standard 61000-4-2/-4-4). The test voltages are in the kilovolt range. The ICs themselves have considerably lower disturbance levels. The pulse voltages which are applied to the device from outside are attenuated on their way through the assembly. Voltages of several kilovolts outside the device are thus measured as only 1 to 100 V on the IC pin. The IC test system (figure 2) has thus been developed to test the IC immunity to pulse disturbances. The IC test system lets the user of ICs keep track of changes in disturbance immunity and document these, take control over component selection and layout and make decisions on where to use the IC. The IC test system lets manufacturers of ICs check the disturbance immunity of existing ICs, and identify the causes of distur-

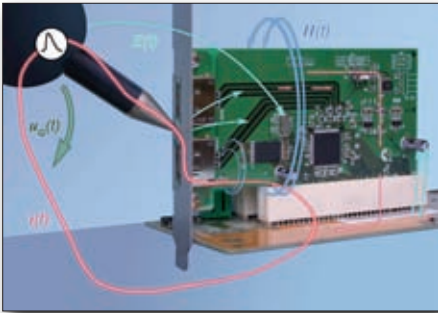


Figure 1. Typical ESD test set-up



Figure 2. System for testing IC immunity to pulse disturbances

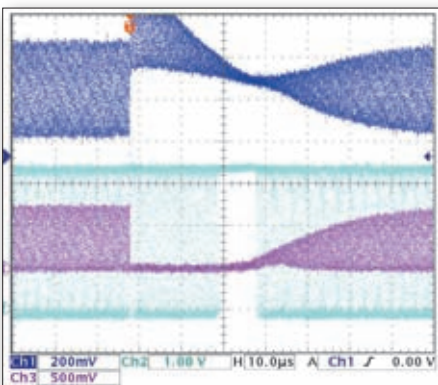


Figure 3. Signal behaviour on oscillator crystal and PLL during disturbance coupling

bances and optimise the IC.

The generators from the P200 and P300 series are provided for disturbance pulse coupling. They are dimensioned according to the mechanisms used for coupling pulses into electronic assemblies. Generators from the P200 series are provided to generate disturbances by pulse magnetic fields. These generators have a high coupling capacitance and a low resistance and inject a high current with a short rise time into the IC pin. They are used to simulate the induction loops which may occur on a finished board. In extreme cases, these induction loops may comprise the IC's internal current path and a blocking capacitor which is connected to the pin. Generators from the P300 series are used to simulate disturbances caused by pulse electric fields. They have a high resistance and a small coupling capacitance. The generators from the P300 series simulate the dis-

placement current coupling of the electric field, and couple voltage pulses whose short rise time is similar to the P200 series into the IC pin. The generators are controlled by a special supply station (BPS 201).

It is common for manufacturers to discontinue production of the IC types used in an existing application. The successor type has been shrunk (reduction of the structural width) for reasons of costs and probably revised in terms of technology. Although it is pin-compatible and has gained more functional features, its disturbance immunity characteristics may also be worse. Such changes may entail high costs if this IC is used in not just one assembly but several applications. Standard measurements have to be carried out which result in new development work through changes to the layout design and additional production costs if the test is not passed. Table 1 shows such a practical example. The manufacturer has replaced the predecessor IC (yellow columns) that was used in more than 80 applications with a shrunk successor IC (red columns). The result of device tests with the ESD generator from Schaffner was one-third worse than the defined limit value of 6kV on average only when the IC was replaced with the engineering sample (customer prototype).

IC areas susceptible to disturbances could be located by the respective functional faults in tests of the immunity to pulse disturbances with the Langer IC test system. Some susceptible pins are listed with their associated fault threshold value for positive (+) and negative (-) disturbances and the type of fault at the bottom of table 1. The fault threshold values of the engineering sample are partly reduced by the factor 10. The results that could be achieved in close cooperation with the IC manufacturer were generally better, due to repeated IC modifications, than with the predecessor design (green columns). The final product used for the application increased the disturbance immunity to such an extent that interference could no longer be detected with the NSG435 standard generator (maximum 9kV).

The signal interference threshold value of data interfaces can cause data errors through the input cells located at the IC pin. These errors are generally remedied by error detection and correction mechanisms that are implemented in the IC. An interference with oscillator or PLL cells causes a clock pulse failure for a matter of nanoseconds or microseconds in a simple case. All processes that depend on a correct timing basis are disturbed. This leads to gaps in data transfer which in turn cause data errors in data communications systems. Clock failure may cause crashes in certain ICs (control sequence error). The crystal oscillating voltage

	predecessor IC		shrunk successor IC					
	used in serial production		engineering sample		final modification			
	fault threshold	type of fault	fault threshold	type of fault	fault threshold	type of fault		
ESD device test with generator NSG435		[kV]		[kV]		[kV]		
	+	5.0	function failure	4.0	function failure	> 9.0	--	
	-	6.0	function failure	4.0	function failure	> 9.0	--	
pulse disturbance of pins with P200/300		[V]		[V]		[V]		
	VDD (3.3V)	+	> 25.0	--	3.1	reset	> 25.0	--
		-	15.0	data failure	5.0	reset	> 25.0	--
VDD PLL (1.8V)	+	> 25.0	--	19.0	data failure	> 25.0	--	
	-	4.5	data failure	2.0	ESD protection	3.0	data failure	
VDD CLK (1.8V)	+	> 25.0	--	10.8	reset	> 25.0	--	
	-	> 25.0	--	1.8	reset	> 25.0	--	
CLK in	+	> 140.0	--	3.5	clock failure	> 140.0	--	
	-	60.0	clock failure	1.5	reset	60.0	clock failure	
CLK out	+	> 140.0	--	10.0	ESD protection	> 140.0	--	
	-	42.0	clock failure	13.0	ESD protection	> 140.0	--	
data line	+	97.0	data failure	14.0	reset	> 140.0	--	
	-	120.0	data failure	56.0	data failure	100.0	data failure	

Table 1. Comparison of disturbance immunities of the same IC product family

is displaced beyond the operating point (Ch1), so that the clock fails on the crystal circuit output (Ch3) if such a disturbance occurs on an oscillator crystal pin (figure 3). The downstream PLL bridges the clock failure temporarily. The PLL also stops for approximately 10µs (Ch2) after the bridging time. In the simplest case the processor stops briefly but restarts after the PLL break. All time-dependent processes are disturbed. Data errors occur in the interfaces. But the PLL clock interruption can also lead to a system crash.

Reset cells can trigger a reset under the influence of disturbances. An incomplete reset may be triggered and results in a crash if the internal reset pulses are too short. ESD protective structures are used to prevent destruction by ESD during handling. Disturbance pulses can cause power clamps, for example. The supply voltage is short-circuited. A reset and restart is triggered if the voltage falls below the reset threshold value. The IC could be de-

stroyed if the power clamps are permanently conductive. A transient is initiated and causes a Vdd dip when current or magnetic field pulses enter the Vdd/Vss supply system. These dips can be identified by internal monitoring (reset). External monitoring, however, fails and cannot trigger a reset either. The voltage dip in the supply system means that the cells suffer an information loss which may possibly result in an uncontrolled crash.

This example clearly shows how IC EMC characteristics are reflected by the device behaviour. Since the disturbance immunity of PCBs and electronic devices will become increasingly important in the future, it is crucial for both the IC manufacturer and the IC user to find compatible solutions through more precise fault analysis. This is the only way for smaller silicon structures to gain economic advantage. The time and money needed to avoid faults can be planned, and the risk thus becomes controllable. ■