

# Design Methods Implicating Electromagnetic Compatibility for Systems in Package

Gerhard Loipold<sup>1</sup>, Bernd Deutschmann<sup>1</sup>

<sup>1</sup>austriamicrosystems AG, Schloss Premstaetten, A-8141 Unterpremstaetten, Austria  
gerhard.loipold@austriamicrosystems.com  
bernd.deutschmann@austriamicrosystems.com

**Abstract** — The increasing design complexity of modern Systems in Package (SiP) together with the trend of using deep submicron technologies results in an additional demand to design ICs in order to satisfy the Electromagnetic Compatibility (EMC) requirements. The wide range of complex analog and digital system building blocks, which are integrated into one package, often cause high electromagnetic emissions. Due to the cost aspects regarding to mobile phones and other portable devices, shielding of ICs on the PCB is in many cases not acceptable and as a result, the electromagnetic emission of integrated circuits must be reduced. This paper provides an overview of design methodologies for achieving the EMC of devices implemented in SiP technologies. It exhibits the importance to imply EMC issues in the early design phase to reduce electromagnetic emissions. Design methods applied to the system design, especially partitioning of the functional blocks, clock tree planning, and power distribution are demonstrated.

## 1. INTRODUCTION

Many of today's embedded systems consist of an analog front-end realized together with a high performance digital system including embedded microcontroller subsystems. Often these digital subsystems are operating at high frequencies, and therefore are the origin of parasitic electromagnetic emissions. The IC customer is no more willing to put additional external components onto the PCB to meet the prescribed EMC requirements. This additionally forces IC designers to take special care about the electromagnetic emission and the susceptibility of their products. But the topic of design optimization for improving the EMC not only affects the design of the IC. It affects the whole design flow starting with the system architecture, the design and layout implementation, and also the design of the SiP substrate PCB.

Generally analog CMOS processes have limits on digital gate density and power consumption, whereas digital deep submicron processes have the disadvantage of an increased leakage current consumption. In many cases the different demands of having high performance analog and digital systems can not be fulfilled by one silicon process. Therefore splitting the analog and digital functionality into two different dice is preferred. A commonly used design flow for SiPs comprises the partitioning of the overall system function into several function blocks. These function blocks are divided to several analog and digital blocks. Further, the digital system function is divided to HW and SW. In order to

enable a good noise decoupling the analog and the digital blocks are located on separated dice. The analog functions are implemented with a high performance low noise mixed signal process, while the digital functionality is implemented with a high speed deep submicron digital process characterized by optimum gate density and minimum power consumption. The analog front-end together with the digital system are mounted onto a multi-layer substrate PCB and packaged into a so-called "Multi-Chip-Module" (MCM) (see Fig. 1).

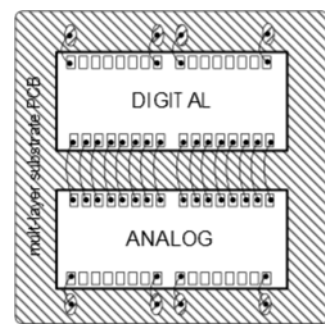


Fig. 1. Example of a Multi-Chip-Module; digital and analog die mounted onto a substrate PCB

## 2. ROOT CAUSES FOR ELECTROMAGNETIC EMISSIONS OF SiPs

SiPs often show a variety of different root causes for high conducted and the radiated electromagnetic emissions if they are not designed with respect to EMC. In most cases many different sources are responsible for the emissions. Disturbances are often caused by simple circuit blocks (e.g. I/O drivers, clock tree buffers, logic gates) producing high current peaks. The sum of these current peaks is flowing in loop antennas formed by the VDD and VSS paths on the die. Due to partitioning the system into two separated dice additional sources of the electromagnetic emission are generated. The main sources are the interfaces with large input and output buffers between these two dice, which act as emitters for the electromagnetic energy together with high frequency currents that are flowing across the interfaces between the analog and the digital die. Due to insufficient on-chip decoupling capacitances high frequency currents flowing across the global VDD and VSS busses on the substrate PCB are generated and responsible for an increasing fraction of electromagnetic emission.

Another root cause of the electromagnetic emission is ground bouncing. Ground bouncing is caused by transient current peaks flowing across the parasitic inductances in the ground path (i.e. self- and mutual inductances of the loops formed by the bond wires and lead frames). The sudden current change across the inductance results in a voltage drop, which shifts the voltage potential of the dice. This voltage shift causes common mode currents, which are further responsible for high emissions. A ranking list of the main origins of the electromagnetic emissions is shown in Table 1.

TABLE I  
RANKING LIST FOR THE EMISSIONS

Source of Disturbance	Severity
Large peripheral output drivers	high
Large peripheral input buffers	high
Large clock tree buffers	medium
Core logic gates with high fan out	medium
Data busses	low
Analog parts	low

The electromagnetic emissions are amplified by:

- Power supply busses that are forming loop antennas
- Parasitic inductance responsible for ground bouncing
- Insufficient on-chip decoupling capacitances
- Current surges flowing between the digital- and the analog die
- Current loops formed by the substrate PCB

### 3. ELECTROMAGNETIC EMISSION MEASUREMENT METHODS

To find the root cause of the electromagnetic emissions of SiPs the following measurement methods can be used. To demonstrate these different measurement methods several EMC investigations were performed based on an embedded system. This embedded system comprises all the digital and analog functionality of a digital audio player onto one MCM (see Fig. 2). The full synchronous digital part has a complexity of some 100k gate equivalents. The analog part mainly consists of an ADC and a DAC, an oscillator, a PLL, and an USB physical interface. The power supply of the digital part is provided by two integrated voltage regulators (LDO) which are located on the analog die.

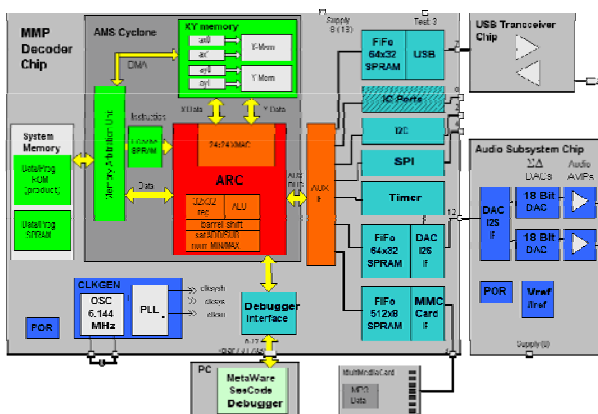


Fig. 2. Block diagram of the MCM digital audio player

### 3.1 Setup for EMC Measurements

The EMC analyses were performed by the means of three measurement methods:

- Radiated electromagnetic emission measurement according to IEC 61967-2 (TEM-Cell method) [1]
- Near magnetic field measurement using a special near field probe in a small frequency range
- Surface scan of the dice and the MCM package at one specific frequency according to IEC 61967-3 [2]

With the help of the explained measurement methods multiple root causes of electromagnetic emissions of the digital audio player were found. In the following chapters several design guidelines to eliminate these root causes are discussed.

#### 3.1.1 TEM-Cell Measurement

To get an overview of the total electromagnetic emission of the digital audio player, the radiated emission was measured using a TEM-Cell. In Fig. 3 the standardized emission level scheme is shown for the frequency range of 150 kHz to 1 GHz. The figure shows the radiated emission (maximum) together with the classification of emission levels (max. emission). For this example the maximum emission can be classified with "H7". This result gives useful information about critical frequencies which have to be further analyzed. The drawback of this method is that no specific information is given about the emission source.

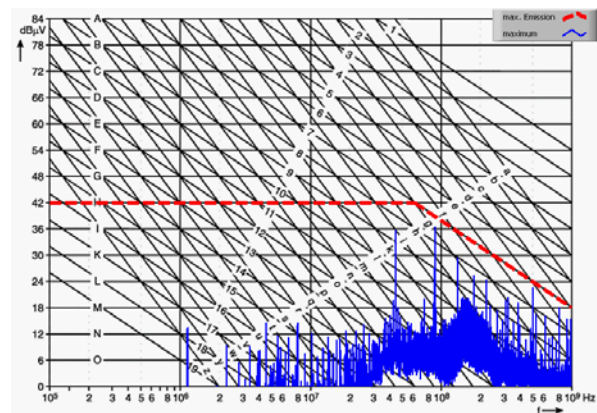


Fig. 3. Radiated electromagnetic emission spectrum

#### 3.1.2 Near Magnetic Field Measurements

To further analyze the critical frequency bands (e.g. GSM1800) a magnetic field probe (Langer RFB0.3-3) [3] was used. The probe was placed in a constant distance of  $d=1$  mm to the surface of the IC package. The area of the IC has been screened in x- and y-direction with a step size of  $D=2$  mm. At every cross point  $M_{xy}$  of the screening matrix (see Fig. 4) the near magnetic field component was measured. With a package size of  $A=100$  mm<sup>2</sup> 36 measurement points had to be analyzed. The collection of the measurement results gives further information about the distribution of the magnetic field and yields first localizations of the emission sources.

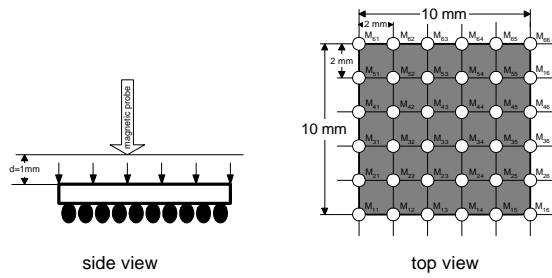


Fig. 4. Setup for the near field measurements at the surface of the MCM package

The diagram in Fig. 5 shows the radiated electromagnetic emission at the measuring point  $M_{22}$  in the GSM frequency range between 1710 MHz and 1880 MHz. At 1720 MHz and 1810 MHz two peaks with higher emission were figured out.

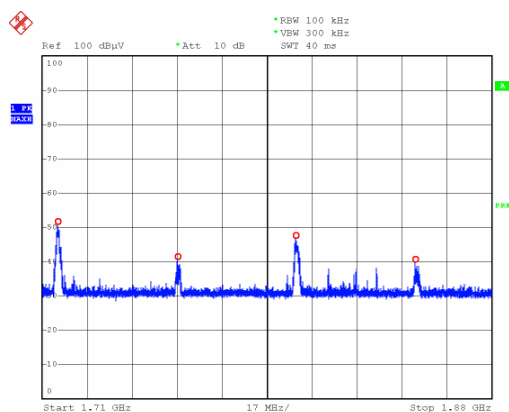


Fig. 5. Measurement result of the digital audio player at the measuring point  $M_{22}$

### 3.1.3 Surface Scan in a Small Frequency Band

To localize the root cause of the high electromagnetic emission that was found in the previous measurements at 1720 MHz, a surface scan of the whole MCM was performed. In this case a high-resolution magnetic field probe was automatically moved with a very small step size of 50  $\mu\text{m}$  in x- and y-direction over the MCM package (see Fig. 6).

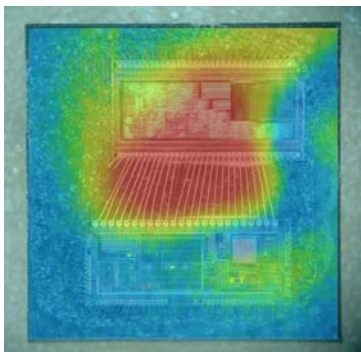


Fig. 6. Surface scan result at 1720MHz over the MCM package

This measurement method provides a more detailed distribution of the emission and helps detecting functional building blocks with high electromagnetic activity. Together with the GDSII layout data the

aggressors down to gate level can be localized. In this case the maximum magnetic field was found over the digital die and the interface between the digital and the analog dice. The hot spots show the context between local appearances of circuit blocks which are the root cause of the electromagnetic emission.

More detailed information about the magnetic field distribution can be obtained by scanning the surface of the two dice separately (see Fig. 7). The hot spots are located over some large buffers of the clock tree on the digital die as well as the high frequency switching output cells on the digital and the analog die.

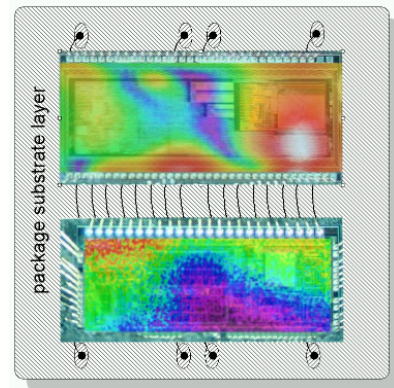


Fig. 7. Surface scan result at 1720MHz

## 4. DESIGN RULES FOR IMPROVED EMC

### 4.1 Package Substrate Circuits for MCMs

Usually SiPs are powered by integrated voltage regulators (LDO) placed on the analog die. The power nets (e.g. bond wires and metal traces) are often routed via the package substrate circuit board from the voltage regulator of the analog die to the digital die. These power nets often cause additional parasitic inductances by forming loop antennas. Avoiding these loop antennas is one of the most important design measure for good EMC. A convenient method to avoid power loops in SiPs is the usage of a multi-layer substrate circuit board. With a multi-layer substrate as shown in Fig. 8c additional layers can be used for signal routing and low impedance VSS and VDD planes are offered for the power distribution. For the substrate PCB layouts the following design rules should be considered:

- Route the VDD and VSS traces in parallel close together especially for 2- layer substrates.
- Implement a separate VSS and VDD power plane for 4-layer substrates.
- Place the VDD and VSS balls next to each other (this enables the PCB designer to place decoupling capacitors with minimum routing).
- Use die-to-die bonding for fast interface signals.
- The external VDD and VSS supply balls should be located close to the supply pads of the dice.

Fig. 8 shows step-by-step in which way the EMC of a package substrate circuit can be improved by applying the design rules mentioned above.

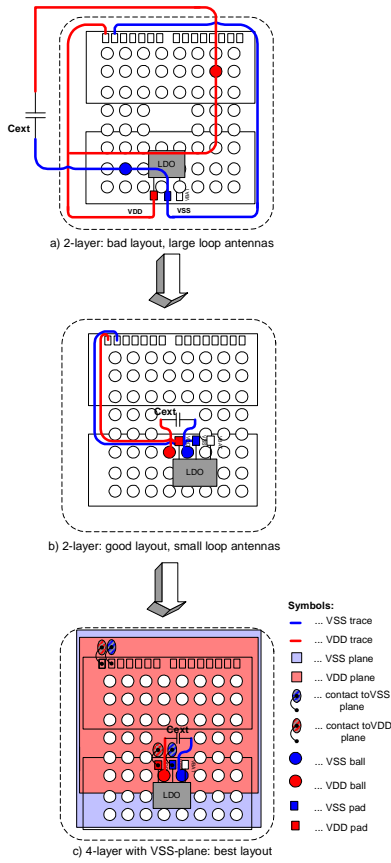


Fig. 8. Several substrate PCB layouts variants

## 4.2 Floor planning of the pads

To ensure an EMC optimized substrate layout the VDD and VSS pads should be placed nearby their voltage source e.g. the LDO output of the analog die. To decrease the parasitic inductances of the power net additional VDD and VSS pads and multiple bonding wires can be used. To estimate the right amount of VSS pads the amplitude of the ground bounce noise  $V_{n1,2}$  which is caused by the crowbar current of the output drivers can be predicted using (1) with  $V_K = V_{IN} - V_{TN}$ ,

$$V_{n1,2} = V_K + \delta \cdot \left( 1 \pm \sqrt{2V_K \frac{1}{\delta} + 1} \right) \quad \delta = \frac{mT}{L_{VSS1} n \beta_N} \quad (1)$$

where (m) is the number of VSS pads, (n) is the number of output drivers switching simultaneously, ( $L_{VSS1}$ ) is the lumped inductance of one VSS path, ( $\beta_N$ ,  $V_{TN}$ ) are transistor parameters of the output driver, ( $V_{IN}$  and  $V_{DD}$ ) are the input and the supply voltage, and T is the time it takes for the switching current to reach its peak value.

## 4.3 Routing of Supply Busses for Large Digital Systems

Conventional power routing for the core logic cells is often done by a global power ring around the core. Several horizontal VDD and VSS busses connected to the global power ring on the right and left hand side are used to supply the core logic cells of one row. Each cell of one row is therefore only supplied by one horizontal VDD

and VSS bus trace. As each row includes a local decoupling capacitance that is mainly supplying the cells within the row, all the other cells of the surrounding rows can not be properly supplied by this decoupling capacitance. This makes the local on-chip decoupling less efficient.

A grid matrix for the VDD/VSS supply network provides a more homogenous distribution of the current flow in all locations. Therefore on-chip decoupling capacitances from one row can also provide decoupling for cells from another row. The power concept, the decoupling, and therefore the EMC can be improved by using a grid matrix supply network as illustrated in Fig. 9. The additional vertical metal traces with their parasitic metal-to-metal capacitances contribute to the total on-chip decoupling capacitance between the VDD and VSS supply. This decoupling capacitance can further be increased by routing the VDD and VSS bus traces with a minimum distance on top of each other instead of side by side.

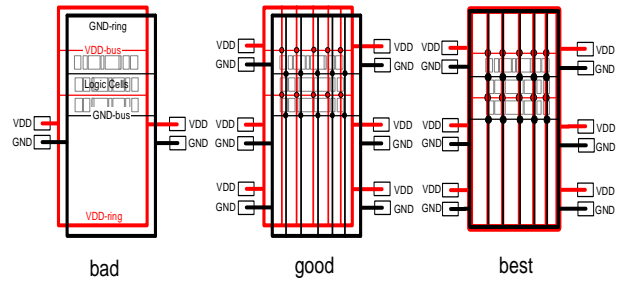


Fig. 9. Power routing concepts

## 4.4 On-Chip Decoupling (OCD)

OCD capacitances between the VDD and VSS supply rails act as charge reservoirs that supply the chip and thus help smoothing the voltage transients. In addition they keep the high dynamic current surges ( $di/dt$ ) inside the chip.

There are several ways to implement on-chip decoupling capacitance into an IC.

The question which type of capacitance shall be used is mostly driven by the available space and cost factors. It is strongly recommended to add some on-chip decoupling capacitances close to the cells which are responsible for high current surges.

The most common design measures are:

- Fill empty spacer- and filler-cells with on-chip decoupling capacitances.
- Route VDD and VSS power rails as wide as possible and on the top of each other.
- Allocate additional area of silicon for on-chip decoupling capacitances (e.g. gate caps, poly caps, metal to metal caps,...).

To increase the effectiveness of on-chip decoupling and to further smooth the  $di/dt$  current surges outside of the IC damping resistors should be added to the VDD power rails, e.g. nearby the supply pads.



#### 4.5 Clock Tree Planning for Digital Systems

The clock distribution network, containing an oscillator and the clock tree is one of the most energy consuming circuit parts. In modern SiPs it is estimated that up to 40% of the overall power is consumed by the digital clock tree [4]. The timing of the clock tree is constrained according to the design requirements to keep the clock skew of leaf pins to a minimum. To achieve the typical clock skews of less than 100 ps it is necessary to switch many clock buffers nearly at the same time, which results in high dynamic current peaks over the VDD and VSS power rails.

As conventional clock tree generation tools do not consider EMC issues, the digital designer has to take care of the overall driver size of the clock tree. For good EMC and also to reduce the power consumption it is recommended to avoid over sizing the buffers in the clock tree. RTL power optimization can be used to add additional gating logic in order to turn off functional blocks, which further reduces the switching activity.

Fig. 10 shows a comparison of a conventional and an EMC optimized clock tree. Due to smaller buffers and additional delay elements as gating cells the insertion delay of the clock network will be increased. The tradeoff between clock insertion delay and electromagnetic emission has to be taken into account.

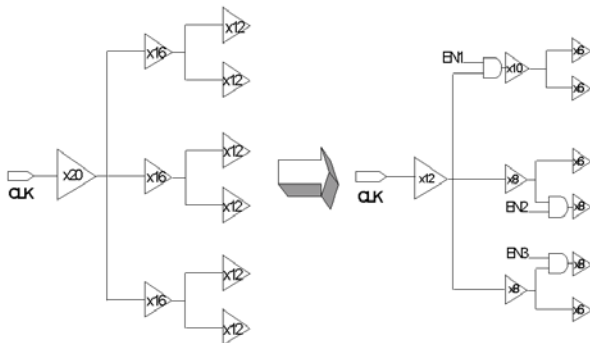


Fig. 10. Conventional vs. EMC optimized clock tree

Before physical implementation the  $di/dt$  of the dynamic current consumption for the whole clock tree network can be estimated by post-layout simulations with a fast SPICE-simulator. The SPICE-netlist includes all driver transistors, RC-parasitics and loads. The simulation result shall be the basis for the decision whether a further optimization of the clock tree has to be done.

Fig. 11 illustrates the current simulation results of the digital audio player's clock tree. High current peaks of up to 290mA and high dynamic current surges with a  $di/dt$  of more than 250mA/ns can be seen. These sharp current surges can result in high electromagnetic emissions over wide frequency ranges.

By optimizing the clock tree the dynamic current peaks could be reduced by a factor of 2 while the insertion delay of the clock network was increased by only 400ps.

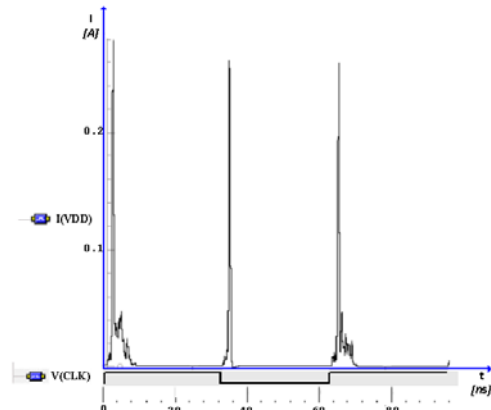


Fig. 11. Clock tree simulation result

In addition the electromagnetic emission was significantly reduced while the functionality of the digital audio player was not influenced. The measurement result of the emission shown in Fig. 12, compared to Fig. 5, demonstrates this improvement.

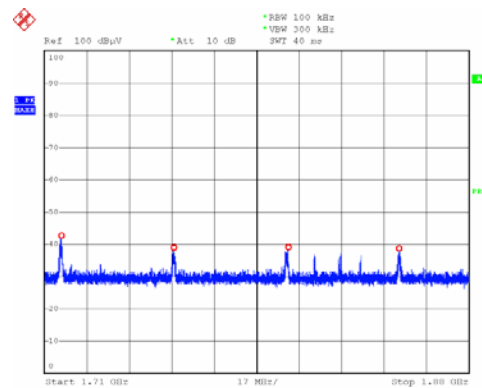


Fig. 12. Electromagnetic emission spectrum of the digital audio player with redesigned clock tree

#### 4.6 Design of Digital Interfaces

The high-speed data exchange between the digital and the analog die has also to be considered for an EMC optimized SiP design. Especially the interfaces of the ADC, the DAC, together with the control interfaces can be the reason of high emissions. High current peaks flowing between the analog and the digital die in conjunction with loop antennas that are formed by the bond wires and the substrate PCB produce high electromagnetic emission. To increase the EMC performance of such die-to-die interfaces it is recommended to avoid high speed serial data transmission. Advanced parallel interfaces with moderate transfer rates should be preferred. Bus encoding (e.g. Gray) can be used to reduce the switching activity by minimizing the number of signal transitions.

With bus skewing of synchronous busses the switching times of the output drivers are delayed by some ns [5]. This spreads the high dynamic switching currents and smoothes the transient current consumption of output drivers, as shown in Fig. 13.

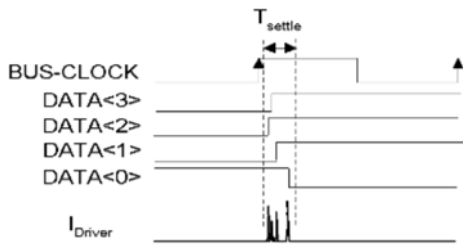


Fig. 13. Bus skewing of the digital interface

#### 4.7 Periphery Cells

Conventional peripheral cells usually produce high dynamic switching currents and therefore high electromagnetic emissions. Especially all pins which are switching at high frequencies as the clocks or the interfaces (e.g. SPI, MMC) are mainly responsible for an increased electromagnetic emission of SiPs.

##### 4.7.1 I/O Cells

For SiPs conventional I/O cells with a combined output and input structure are often used. The input structure is often directly connected to the output drivers. In this case the input drivers are switching synchronously with the output drivers and therefore are also producing switching currents. If the I/O cell is used in the output direction, the input structure should be turned off in order to avoid additional current surges. Fig. 14 gives an example of a conventional and an EMC optimized I/O cell.

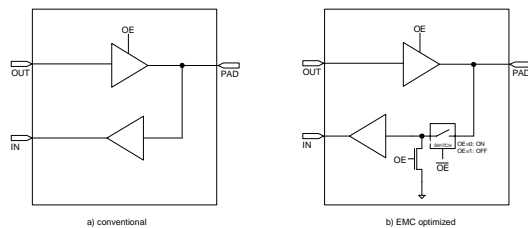


Fig. 14. Conventional vs. EMC optimized I/O cell

##### 4.7.2 Output Cells

The selection of the output drivers which are driving clock signals or high frequency interfaces should be done under the following criteria:

- Minimum driving capability
- Crowbar current elimination
- Slew rate controlled output driver
- Dynamic switching current reduction

In [6] it is shown that the electromagnetic emission as well as the ground bounce noise can significantly be reduced by using EMC improved output drivers. Often such output drivers provide the capability to control the slew rate, the dynamic switching current, and the reduction of the ringing of the output signal.

##### 4.7.3 Input Cells

Conventional input drivers often consist of a level shifter, a Schmitt trigger, and an input buffer. All these components, especially the input buffer, contribute to the dynamic switching current. For SiPs the input drivers shall be selected with the same care as the output drivers.

## 5. RANKING LIST OF DESIGN MEASURES

The ranking list shown in Table II illustrates several design measures in relation to the estimated potential to reduce the electromagnetic emissions.

Additionally the cost factors for silicone area and for the package substrate PCB together with the design efforts are shown.

TABLE II  
RANKING OF DESIGN MEASURES

Measure	Costs	Effort	EME Reduction
On-chip decoupling	medium	high	high
Periphery cells	low	high	high
Optimized substrate PCB (4 layer)	high	high	medium
Clock tree	low	medium	medium
Floor planning of the pads	low	low	medium
Routing of supply busses	low	medium	low
Design of digital interfaces	medium	high	low
Optimized substrate PCB (2 layer)	low	low	low

## 6. CONCLUSION

High electromagnetic emission of systems in package is often the reason for re-designs of ICs and therefore increases the time until final production ramp up. Some of the root causes for high electromagnetic emissions of SiPs were described in this paper. Several measurement techniques to localize the sources of the electromagnetic emissions, as well as some important design rules for improving the EMC of SiPs were demonstrated. The importance of realizing EMC design issues to reduce the electromagnetic emission to a tolerable limit already in the early design phase was emphasized. If EMC awareness is taken into account the time to market can significantly be reduced as no additional redesigns to fulfill the EMC requirements will be needed.

## 7. REFERENCES

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